Heterogeneous Three-Dimensional Electronics by Use of Printed Semiconductor Nanomaterials

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We developed a simple approach to combine broad classes of dissimilar materials into heterogeneously integrated electronic systems with two- or three-dimensional layouts. The process begins with the synthesis of different semiconductor nanomaterials, such as single-walled carbon nanotubes and single-crystal micro- and nanoscale wires and ribbons of gallium nitride, silicon, and gallium arsenide on separate substrates. Repeated application of an additive, transfer printing process that uses soft stamps with these substrates as donors, followed by device and interconnect formation, yields high-performance heterogeneously integrated electronics that incorporate any combination of semiconductor nanomaterials on rigid or flexible device substrates. This versatile methodology can produce a wide range of unusual electronic systems that would be impossible to achieve with other techniques.

Many existing and emerging electronic devices benefit from the heterogeneous integration of dissimilar classes of semiconductors into single systems, in either two-dimensional (2D) or 3D layouts (1, 2). Examples include multifunctional radio-frequency communication devices, infrared imaging cameras, addressable sensor arrays, and hybrid silicon complementary metal oxide semiconductor (CMOS) circuits and nanowire devices (3–7). In some representative systems, compound semiconductors or other materials provide high-speed operation, efficient photodetection, or sensing capabilities; the silicon CMOS provides digital readout and signal processing in circuits that often involve stacked 3D configurations. Wafer- or chip-scale bonding (1, 2, 6–10) and epitaxial growth (3, 7, 12) represent the two most widely used methods for achieving these types of integrated systems.

The bonding processes use fusion processes (8, 9) or layers of adhesives (6, 10) to combine integrated circuits, photodiodes, or sensors formed separately on different semiconductor wafers. This approach works well in many cases, but it has important drawbacks (1, 9), including (i) limited ability to scale to large areas (i.e., larger than the wafers) or to more than a few layers in the third (i.e., stacking) dimension; (ii) incompatibility with unusual materials (such as nanostructured materials) and/or low-temperature materials and substrates; (iii) challenging fabrication and alignment for the through-wafer electrical interconnects; (iv) demanding requirements for planar bonding surfaces; and (v) bowing and cracking that can occur from mechanical strains generated by differential thermal expansion and contraction of disparate materials. Epitaxial growth provides a different approach, which uses molecular beam epitaxy or other means to form thin layers of semiconductor materials directly on the surfaces of wafers of other materials. Although this method avoids some of the aforementioned problems, the requirements for epitaxy place severe restrictions on the quality and type of materials that can be grown, even when buffer layers and other advanced techniques are used (1, 13).

By contrast, nanoscale wires, ribbons, membranes, or particles of inorganic materials, or carbon-based systems such as single-walled carbon nanotubes (SWNTs) or graphene sheets (14–17), can be grown and then suspended in solvents or transferred onto substrates in a manner that bypasses the need for epitaxial growth or wafer bonding. Recent work has shown the integration of isolated crossed nanowire diodes in 2D layouts formed by solution casting (18). Our results show how dissimilar single-crystal inorganic semiconductors (such as micro- and nanoscale wires and ribbons of GaN, Si, and GaAs) can be combined with one another and also with other classes of nanomaterials (such as SWNTs) with the use of a scalable and deterministic printing method to yield complex, heterogeneously integrated electronic systems in 2D or 3D layouts. The capabilities of this process are demonstrated by ultrathin multilayer stacks of high-performance metal oxide semiconductor field-effect transistors (MOSFETs), high electron mobility transistors (HEMTs), thin-film transistors (TFTs), photodiodes, and other components that are integrated into device arrays, logic gates, and actively addressable photodetectors on rigid inorganic and flexible plastic substrates.

Figure 1 illustrates representative steps for producing these types of systems. The process begins with the synthesis of the semiconductor nanomaterials, each on their own source substrate. The devices shown in Fig. 1 allow micro- and nanoscale wires and ribbons of single-crystalline GaN, GaAs, and Si that were formed with the use of wafer-based source materials and lithographic etching procedures (19–23) to be integrated with each other or with networks of SWNTs that were grown by chemical vapor deposition (16, 23). Scanning electron micrographs at the top of Fig. 1 show these semiconductor nanomaterials after their removal from the source substrates. For circuit fabrica-
tion, these elements remain in the configurations defined on the wafers during the fabrication or growth stage: aligned arrays in the case of the GaN, GaAs, and Si materials, and monolayer random networks for the SWNTs. High-temperature doping and annealing procedures for ohmic contacts to the GaN, GaAs, and Si can be performed on the source substrates.

The next step involves transferring these processed elements, with the use of an elastomeric stamp-based printing technique (19), from the source substrates to a device substrate, such as a sheet of polyimide (PI) (Fig. 1). In particular, laminating a stamp of polydimethylsiloxane against the source substrate establishes soft, van der Waals adhesion contacts to the semiconductor nanomaterial elements. We contacted the “inked” stamp to a device substrate (such as a PI sheet) with a thin, spin-cast layer of a liquid prepolymer (such as polyamic acid) on its surface and then cured the polymer, which left these semiconductor materials embedded on and well adhered to this layer (19–22) when the stamp was removed. Similar procedures work well with a range of substrates (i.e., rigid or flexible and organic or inorganic) and semiconductor nanomaterials. We used a slightly modified version of this process for the SWNT devices (23). The thickness of the interlayer (PI in this case) can be as small as 500 nm and was typically 1 to 1.5 μm for the systems we describe.

After some additional processing—including deposition and patterning of gate dielectrics, electrodes, and interconnects—the transfer printing and device fabrication steps can be repeated, beginning with spin-coating a new prepolymer interlayer on top of the previously completed circuit level. Automated stages specially designed for transfer printing or conventional mask aligners enable overlay registration accuracy of ~2 μm over several square centimeters (fig. S1). The spatial distortions associated with the printing had a mean value of ~0.5 μm (fig. S2). The yields for printing of Si, SWNT, GaAs, and GaN were >99%, >99%, >95%, and >85%, respectively. Defects in these last two cases were associated with fracture and imperfection for the relatively wide GaAs ribbons and relatively thick GaN bars, respectively (fig. S3). Layer-to-layer interconnects (24) were formed simply by evaporating metal lines over and into openings in the interlayers defined by photopatterning and/or dry etching.

This fabrication approach has several important features. First, all of the processing on the device substrate occurs at low temperatures, thereby avoiding differential thermal expansion and shrinkage effects that can result in unwanted deformations in multilayer stacked systems. This operation also enables the use of low-temperature plastic substrates and interlayer materials, and it helps to ensure that underlying circuit layers are not thermally degraded by the processing of overlying devices.

Second, the method is applicable to broad classes of semiconductor nanomaterials, including emerging materials such as SWNTs. Third, the soft stamps enable nondestructive contacts with underlying device layers; these stamps, together with the ultrathin semiconductor materials, can also tolerate surfaces that have some topography. Fourth, the ultrathin device geometries and interlayers allow easy formation of layer-to-layer electrical interconnects by direct metallization over the device structure. These features overcome many of the disadvantages of conventional approaches.

Figure 2 presents three-layer, 3D stacks of arrays of Si MOSFETs fabricated by the general process flow shown in Fig. 1. We used single-crystalline silicon nanoribbons with doped contacts (formed on the source wafer), SiO2 dielectrics formed by plasma-enhanced chemical vapor deposition, and Cr/Au metallization for the source, drain, and gate electrodes (25). Each device uses three aligned nanoribbons, each with length _L_ = 250 μm, width _W_ = 87 μm, and thickness = 290 nm. Figure 2A shows an optical micrograph of an edge of the system; the layout of the system was designed to reveal separately the parts of the substrate that support one, two, and three layers of MOSFETs. A 90° rotation of the device geometry for the second layer, relative to the first and third, helps to clarify the layout of the system. Schematic cross-sectional and angled views of the stacked structure are shown in Fig. 2B. The sample can be viewed in 3D using confocal optical microscopy. Figure 2C shows top and angled views of such images. (The image quality degrades somewhat with depth because of scattering and absorption from the upper layers). Figure 2D presents electrical measurements of representative devices in each layer. Devices on
each of the three layers, which are formed on a PI substrate, show excellent properties with linear mobilities of 470 ± 30 cm²/Vs (where the error is SD), on/off ratios greater than 10⁶, and threshold voltages of -0.1 ± 0.2 V; there are no systematic differences between devices in different layers. Additional layers can be added to this system by repeating the same procedures. To investigate issues related to mismatches in coefficients of thermal expansion in these systems, we evaluated the behavior of the devices under thermal cycling (60 times) between room temperature and 90°C. Small changes were observed for the first few cycles followed by stable behavior (fig. S9).

In addition to 3D circuits with a single semiconductor, Fig. 3 illustrates that the capability to combine various semiconductors can be used in multiple layers. We fabricated arrays of HEMTs, MOSFETs, and TFTs—with the use of GaN bars, Si nanoribbons, and SWNT films, respectively, on PI substrates. Figure 3, A and B, shows high-magnification optical and confocal images, respectively, of the resulting devices. The GaN HEMTs on the first layer use ohmic contacts (Ti/Al/Mo/Au, annealed on the source wafer) for the source and drain, and Schottky (Ni/Au) contacts for the gates. Each device uses GaN ribbons (composed of multi-layer stacks of AlGaN/GaN/AlN) interconnected electrically by processing on the device substrate. The SWNT TFTs on the second layer use SiO₂ and epoxy for the gate dielectric and Cr/Au for the source, drain, and gate. The Si MOSFETs use the same design as those shown in Fig. 2. Various other devices can be constructed with different combinations of Si, SWNT, and GaN (figs. S4 and S5). Figure 3C presents the current-voltage characteristics of typical devices in the systems of Fig. 3, A and B. In all cases, the properties are similar to those fabricated on the source wafers: The GaN HEMTs have threshold voltages ($V_{th}$) of -2.4 ± 0.2 V, on/off ratios greater than 10⁶, and transconductances of 0.6 ± 0.5 mS; the SWNT TFTs have $V_{th} = -5.3 ± 1.5$ V, on/off ratios greater than 10⁶, and linear mobilities of 5.9 ± 2.0 cm²/Vs; and the Si MOSFETs have $V_{th} = 0.2 ± 0.3$ V, on/off ratios greater than 10⁴, and linear mobilities of 500 ± 30 cm²/Vs.

Another interesting aspect of these devices, which follows from the use of thin PI substrates (25 μm), devices (~1.7 μm), and PI interlayers (1.5 μm), is their mechanical bendability. This characteristic is important for applications in flexible electronics, for which these systems might provide attractive alternatives because of their enhanced capabilities compared with those of conventional organic-based devices. We evaluated the effective transconductance ($g_{m eff}$) for the Si, SWNT, and GaN devices in the system of Fig. 3A as a function of bend radius. Figure 3D, which shows these data normalized to the transconductance in the un bent state ($g_{m0}$), demonstrates the stable performance for bend radii down to 3.7 mm. To explore the response of devices to operation under various conditions, such as repeated bending and electrical testing, we carried out two sets of experiments. Repeated bending (up to 2000 cycles) resulted in no substantial change in the properties of the devices (fig. S8). Repeated electrical testing showed stable responses (~10% changes in properties, or less) (fig. S11). Figures S12 to S15 present information on variation in device properties.

Electrical interconnections formed between different levels in these devices can create

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**Fig. 3.** (A) Optical micrograph of 3D heterogeneous integrated electronic devices, including GaN nanoribbon HEMTs, Si nanoribbon MOSFETs, and SWNT network TFTs, in a three-layer stack. (B) 3D image collected by confocal microscopy. The SWNT TFTs on the second layer use SiO₂ and epoxy for the gate dielectric and Cr/Au for the source, drain, and gate. The SWNT TFTs use the same design as those shown in Fig. 2. Various other devices can be constructed with different combinations of Si, SWNT, and GaN (figs. S4 and S5). Figure 3C presents the current-voltage characteristics of typical devices in the systems of Fig. 3, A and B. In all cases, the properties are similar to those fabricated on the source wafers: The GaN HEMTs have threshold voltages ($V_{th}$) of -2.4 ± 0.2 V, on/off ratios greater than 10⁶, and transconductances of 0.6 ± 0.5 mS; the SWNT TFTs have $V_{th} = -5.3 ± 1.5$ V, on/off ratios greater than 10⁶, and linear mobilities of 5.9 ± 2.0 cm²/Vs; and the Si MOSFETs have $V_{th} = 0.2 ± 0.3$ V, on/off ratios greater than 10⁴, and linear mobilities of 500 ± 30 cm²/Vs.

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**Fig. 4.** (A) Image of a printed array of 3D silicon n-channel metal oxide semiconductor inverters on a PI substrate. The inverters consist of MOSFETs (channel lengths of 4 μm, load-to-driver width ratio of 6.7, and a driver width of 200 μm) on two different layers, interconnected by electrical via structures. The image on the top right provides a magnified view of the region indicated by the red box in the left frame. The graph on the bottom right shows transfer characteristics of a typical inverter. (B) Transfer characteristics of a printed complementary inverter that uses a p-channel SWNT TFT (channel length and width of 30 and 200 μm, respectively) and an n-channel Si MOSFET (channel length and width of 75 and 50 μm, respectively). The insets provide an optical micrograph of an inverter (left) and a circuit schematic (right). (C) Current-voltage response of a GaAs MSM (channel length and width of 10 and 100 μm, respectively) integrated with a Si MOSFET (channel length and width of 9 and 200 μm, respectively) at different levels of illumination from dark to 11 μW with an infrared light source at 850 nm. The insets show an optical image (left) and a circuit diagram (right). gnd, ground.
interested circuit capabilities. The thin polymer interlayers allow robust interconnects to be formed easily by evaporating metal lines over lithographically defined openings. Thermal cycling tests showed no changes in their properties (fig. S10). Figure 4A shows a 3D n-channel metal oxide semiconductor inverter (logic gate) in which the drive ($L = 4 \mu m$, $W = 200 \mu m$) and load ($L = 4 \mu m$, $W = 30 \mu m$) Si MOSFETs are on different levels. With a supply voltage of 5 V, this double-layer inverter exhibits well-defined transfer characteristics with gains of ~2, comparable to the performance of conventional planar inverters that use similar transistors. Figure 4B shows an inverter with a complementary design (CMOS) with the use of integrated n-channel Si MOSFETs and p-channel SWNT TFTs, designed to equalize the current-driving capability in both pull-up and pull-down directions. Transfer curves collected with a supply voltage ($V_{dd}$) of 5 V and gate voltage (input) swept from 0 to 5 V appear in Fig. 4B. The curve shapes and gains (as high as ~7) are qualitatively consistent with numerical circuit simulations (fig. S6). As a third example, we built GaAs metal-semiconductor-metal (MSM) infrared detectors (26), integrated with Si MOSFETs on flexible PI substrates, to demonstrate a capability for fabricating unit cells that could be used in active infrared imagers. In this case, printed nanoribbons of GaAs ($L = 400 \mu m$, $W = 100 \mu m$, and thickness = 270 nm) transferred onto a substrate with a printed array of Si nanoribbon MOSFETs form the basis of the MSMs. Electrodes (Ti/Au) deposited on the ends of these GaAs nanoribbons form back-to-back Schottky diodes with separations of 10 \mu m. The resulting detector cells exhibit current enhancement as the intensity of infrared illumination increases (Fig. 4C), consistent with circuit simulation (fig. S7). A responsiveness of about 0.30 A/W at the 850-nm wavelength is observed from 1 to 5 V. (This value underestimates the true responsiveness because it ignores optical reflection). The bendability of this system, which is comparable to that of the devices in Fig. 3, could be useful for advanced systems such as curved focal plane arrays for wide-angle infrared night vision imagers.

Printed semiconductor nanomaterials provide new approaches to 3D heterogeneously integrated systems that could be important in various fields of application, including not only those suggested by the systems reported here but also others such as microfluidic devices with integrated electronics, chemical and biological sensor systems that incorporate unusual materials with conventional silicon-based electronics, and photonic and optoelectronic systems that combine light emitters and detectors of compound semiconductor with silicon drive electronics or microelectromechanical structures. Furthermore, the compatibility of this approach with thin, lightweight plastic substrates may create additional opportunities for devices that have unusual form factors or mechanical flexibility as key features.

References and Notes
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Quantum Spin Hall Effect and Topological Phase Transition in HgTe Quantum Wells
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We show that the quantum spin Hall (QSH) effect, a state of matter with topological properties distinct from those of conventional insulators, can be realized in mercury telluride–cadmium telluride semiconductor quantum wells. When the thickness of the quantum well is varied, the electronic state changes from a normal to an “inverted” type at a critical thickness $d_c$. We show that this transition is a topological quantum phase transition between a conventional insulating phase and a phase exhibiting the QSH effect with a single pair of helical edge states. We also discuss methods for experimental detection of the QSH effect.

The spin Hall effect (1–5) has recently attracted great attention in condensed matter physics, not only for its fundamental scientific importance but also because of its potential application in semiconductor spintronics. In particular, the intrinsic spin Hall effect promises the possibility of designing the intrinsic electronic properties of materials so that the effect can be maximized. On the basis of this line of reasoning, it was shown (6) that the intrinsic spin Hall effect can in principle exist in band insulators, where the spin current can flow without dissipation. Motivated by this suggestion, researchers have proposed the quantum spin Hall (QSH) effect for graphene (7) as well as for semiconductors (8, 9), where the spin current is carried entirely by the helical edge states in two-dimensional samples.

Time-reversal symmetry plays an important role in the dynamics of the helical edge states (10–12). When there is an even number of pairs of helical states at each edge, impurity scattering or many-body interactions can open a gap at the edge and render the system topologically trivial. However, when there is an odd number of pairs of helical states at each edge, these effects cannot open a gap unless time-reversal symmetry is broken.

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Figs. S1 to S15
SUPPORTING ONLINE MATERIAL

“Heterogeneous Three Dimensional Electronics by Use of Printed Semiconductor Nanomaterials”

MATERIALS AND METHODS

Printing Process

The printing involves the positioning of a PDMS stamp over a source wafer, establishing contact with this wafer, followed by peeling back to remove the nanostructures and, finally, transfer printing of these structures onto the target substrate. Figure S1 provides an image of a printer designed specifically for this purpose. The fabrication was performed using this system or a commercial mask aligner (Suss Microtech. Inc. MJB3). The reproducibility of the printing process has two aspects: (a) yields with which the structures can be printed onto the target substrate, and (b) absolute and relative positional accuracy of this printing process.

The registration depends on the mechanical accuracy of the stages of the printer and the distortions that can be induced in the PDMS during printing. To investigate these issues, we printed a layer of interconnected Si ribbons, spin cast a polyimide separation layer, and then printed another layer of interconnected ribbons but with an overall, well-defined rotation relative to the first layer. From this bilayer system, we measured the local offsets as a function of position across the printed area, in a point by point fashion, after subtracting the overall rotation. The results define a vector field of offsets. Using these data, we calculated the position averaged magnitude of the offsets. This comparison defines the positioning accuracy of our printer to be ~2 \( \mu \text{m} \). Next, we subtracted a rigid overall translation from the vector field of offsets to reveal the underlying random distortions associated with the printing process. We find that these distortions have a distribution that is random across the printed area, with an average magnitude of ~0.5 \( \mu \text{m} \). Figure S2 summarizes this information. These results, while sufficient for many applications, do not represent fundamental limits. Increasing the engineering sophistication of the stages (e.g. using optically encoded stages) and of the stamps (e.g. using designs with rigid backings in composite layouts) can improve the performance.

The yields depend on the type of material, and the geometries of the structures. We find that the yields for the Si, SWNT, GaAs and GaN structures are >99%, >99%, >95% and >85%, respectively. Detailed examination of the printing defects in these second two cases shows that they arise from impartial transfer of the GaN bars, due to their relatively large thicknesses, and fracture of the GaAs ribbons, due to their relatively large widths. These results reinforce a key message of the paper: material structures with nanoscale dimensions are critically important to the printing and integration processes for these systems. Figure S3 shows typical results.
Device fabrication

(a) Silicon devices: The fabrication begins with definition of contact doped thin ribbons of single crystal silicon, by processing silicon on insulator wafer (SOI; Soitec unibond with a 290 nm top Si layer with doping level of 6.0–9.4x10^{14}/cm^3). The first step involved phosphorous doping, using a solid source and spin-on-dopant (Filmtronic, P509), and a photolithographically defined layer of plasma enhanced chemical vapor (PECVD) deposited SiO_2 (Plasmatherm, 300nm, 900mTorr, 350sccm, 2% SiH_4/He, 795sccm NO_2, 250°C) as a mask to control where dopant diffuses into the silicon. After doping, SF_6 plasma etching through a patterned layer of photoresist defined the ribbons. Undercut etching of the buried oxide with concentrated HF solution (Fisher Chemicals) released the ribbons from the wafer. This procedure completed the fabrication of contact doped ribbons of single crystal silicon. In the next step, contacting a flat elastomeric stamp of polydimethylsiloxane (PDMS, A:B=1:10, Sylgard 184, Dow Corning) with the photoresist-coated ribbons and then peeling back the stamp removed the ribbons from the wafer and left them adhered, by van der Waals forces between the hydrophobic PDMS and the photoresist, to the surface of the stamp. The stamp thus ‘inked’ with µs-Si ribbons from wafer was laminated against a polyimide (PI) sheet of 25 µm (Dupont, Kapton100E) spin-coated with a thin layer (~1.5µm) of liquid PI precursor, polyamic acid (Sigma_Aldrich Inc.). Curing the precursor, peeling off the PDMS stamp, and stripping the photoresist left the ribbons embedded on and well adhered to the surface of the PI substrate. The gate dielectric layer consisted of a layer of SiO_2 (thickness ~100 nm) deposited by PECVD at relatively low temperature, 250°C. Photolithography and CF_4 plasma etching defined openings to the doped source/drain regions of the silicon. Source, drain and gate electrodes of Cr/Au (5/100 nm, from bottom to top by electron beam evaporation, Temescal FC-1800) were defined in a single step by photolithography and wet etching.

(b) GaN devices: GaN microstructures were fabricated on a bulk wafer of GaN with heterostructure [ AlGaN(18 nm)/ GaN(0.6 µm)/ AlN(0.6 µm)/ Si]. An ohmic contact area defined by AZ 5214 photoresist and then cleaned with SiCl_4 plasma in a RIE system. A Ti/Al/Mo/Au (15/60/35/50 nm) metal layer was then deposited by e-beam evaporation (Ti/Al/Mo) and thermal evaporation (Au). Washing away the resist completed left metal contacts on the GaN. Thermal annealed at 850 °C for 30 sec in N_2 ambient formed the ohmics. SiO_2 (Plasmatherm, 300nm, 900mTorr, 350sccm, 2% SiH_4/He, 795sccm NO_2, 250°C) and Cr metal (e-beam evaporator, 150 nm) layers were deposited as the mask materials for subsequent inductively coupled plasma (ICP) etching. Photolithography, wet etching, and RIE processing (50 mTorr, 40 sccm CF_4, 100W, 14 min) defined the ribbon geometries of the GaN. After removing the photoresist with acetone, ICP dry etching (3.2 mTorr, 15 sccm Cl_2, 5 sccm Ar, -100V Bias, 14 min) was used to remove the exposed GaN and to etch slightly into the Si (~1.5µm) to facilitate the subsequent anisotropic etching. The Si was then etched away from underneath the GaN using a tetramethyl ammonium hydroxide (Aldrich, 150°C for 4 min 30 sec). The sample was dipped in BOE (6:1, NH_4F: HF) for 30 sec to remove the PECVD SiO_2 and a new 50 nm e-beam evaporated SiO_2 layer was deposited on top of the GaN ribbons. A PDMS slab ‘inked’ with the GaN ribbons from
mother wafer was then laminated against a PI sheet coated with 2 µm polyurethane (PU, Norland optical adhesive, No. 73). The sample was exposed to UV light (173 µWcm⁻²) for 15min to cure the PU. Peeling back the PDMS and removing the e-beam SiO₂ by immersion in BOE for 20sec resulted in the transfer of the GaN elements to the plastic substrate. A negative photoresist (AZ nLOF2020) was used to pattern Schottky contacts of Ni/Au (80/180nm). The photoresist was removed with an AZ stripper (KWIK for 30min).

(c) SWNT devices: Chemical vapor deposition (CVD) was used to grow random networks of individual single walled carbon nanotubes on SiO₂/Si wafers. Ferritin (Sigma Aldrich) deposited on the substrate with a methanol was used as a catalyst. The feeding gas was methane (1900 sccm CH₄ with a 300 sccm H₂). The quartz tube in the furnace was flushed with a high flow of Ar gas for cleaning before growth. During the growth, the temperature was held at 900°C for 20 minutes. The transfer involved either procedures similar to the printing like processes described previously, or a slightly different method in which a thick Au layer and a PI precursor were coated on the SiO₂/Si substrate with the tubes. After curing the PI, the Au/PI was peeled back. Laminating this layer against a prepatterned device substrate coated with a thin epoxy layer (SU8, 150 nm) and then removing the PI and Au layer by oxygen reactive ion etching and wet etching, respectively, completed the transfer. In the case of bottom gate devices, the substrate supported prepatterned gate electrodes and dielectrics. In particular, gate electrodes of Cr/Au/Cr (2/10/10 nm) were patterned by photolithography and then, 300 nm SiO₂ was deposited on the substrate using PECVD. The source and drain electrodes of Cr/Au (2/20nm) were defined directly on top of the tubes.

(d) 3D multilayer stacks of arrays of devices: Sequential application of the processing steps described above can yield stacks of devices in 3D layouts. Figures S4 and S5 give some examples.

3D Circuit

(a) 3D Si NMOS inverter: Multilayer devices were constructed by repetitively applying the same fabrication procedures. In particular, to the PI precursor was spin-cast on the top of an existing layer of devices, and silicon ribbons were transfer-printed on top. The same processes were then used to fabricate devices. For vertical metal interconnects, an electrode area was defined by photo-patterning openings in a layer of AZ4620 photoresist, and then etching away the SiO₂ and PI in this exposed area using CF₄ and O₂ plasma in a RIE system. Depositing 300 nm Al into this area established contacts at the bottom, and provided an electrically continuous connection over the step edge formed by the etched SiO₂ and PI.

(b) SWNT and Si CMOS inverter: The SWNT devices consisted of source/drain contacts of Au (20 nm) defined by photolithography on the tube networks. The SiO₂ (100nm)/Si wafer substrate provided the gate dielectric and gate. Epoxy (SU8, 500 nm) was
then spin-coated onto this substrate after the SWNT transistors were selectively coated with photoresist (AZ5214). After UV exposure for curing of epoxy, a PDMS slab ‘inked’ with undoped Si ribbons was laminated against the substrate and subsequently removed by slow manual peeling to complete the transfer-printing process. Cr/Au (5/100 nm) were used as Schottky contacts for source and drain electrodes in the silicon devices. Al (100 nm) was used to connect the SWNT and Si transistor. See Fig. S6.

(c) GaAs MSM IR detector integrated with Si TFT: GaAs wafers (IQE Inc., Bethlehem, PA.) were used to generate back-to-back schottky diodes. The ribbons were generated from a high-quality bulk wafer of GaAs with multiple epitaxial layers [Si-doped n-type GaAs(120 nm)/semi-insulating(SI)-GaAs(150 nm)/AlAs(200 nm)/SI-GaAs]. The carrier concentration of n-type GaAs is $4 \times 10^{17}$ cm$^{-3}$. GaAs wafers with photoresist mask patterns were anisotropically etched in the etchant (4mL H$_3$PO$_4$ (85 wt%), 52 mL H$_2$O$_2$ (30 wt%), and 48 mL deionized water). The AlAs layers were etched away with a diluted HF solution in ethanol (1:2 in volume). Layers of 2nm Ti and 28nm SiO$_2$ were the deposited by e-beam evaporator. A PDMS stamp inked with the GaAs ribbons was then contacted to a layer of Si transistors coated with PI (thickness 1.5 µm). Peeling back the PDMS and removing Ti and SiO$_2$ by BOE etchant completed the transfer of GaAs to the device substrate. Metals (Ti/Au = 5/70 nm) for the Schottky contacts were deposited by e-beam evaporation. Electrical interconnects between the GaAs back-to-back Schottky diodes and the Si MOSFET were defined by first patterning a layer of AZ4620 photoresist, then etching through the openings using CF$_4$ and O$_2$ plasma in a RIE system and then depositing a 300 nm of Al. See Fig. S7.

Device characterization
A semiconductor parameter analyzer (Agilent, 4155C) and a conventional probing station were used for the electrical characterization of the diodes and transistors. The IR response was measured under IR LED source with wavelength of 850 nM.

Circuit Simulation
To compare the measured transfer curve of the CMOS inverter with a simulation, level 2 PSPICE models for the n-channel Si MOSFET and the p-channel SWNT TFT were generated empirically. These PSPICE models were created based on the default PSPICE MOSFET model (MbreakN and MbreakP) with extracted parameters to fit the measured I-V curves of both Si NMOS and SWNT PMOS shown in Figure S5B. The PSPICE model for GaAs MSM photo-detector was created empirically using back-to-back schottky diodes connected in series with Si MOSFET. See Figs. S6 and S7.

Reliability, Stability and Dispersion in Device Properties

Reliability – Reliability is interpreted to refer to the response of devices to operation under various conditions, such as repeated bending and thermal cycling. To explore this
issue, we carried out two sets of experiments. In the first, we subjected a trilayer stack of Si, GaN and SWNT devices on plastic to 2000 cycles of bending to a radius of curvature of 3.7 mm followed by releasing to a flat, relaxed state. The data from this mechanical fatigue test indicate negligible changes in device behavior. See Fig. S8. In the second set of experiments, we subjected layer to layer electrical interconnects and devices to repeated thermal cycling between room temperature and 90 °C. The interconnects show no change in electrical properties for up to 60 cycles. For devices, we chose to study Si MOSFETs because the mismatch between the coefficient of thermal expansion of Si and the polyimide is the larger than that for the other semiconductor materials explored in this paper, thereby providing the most demanding test of reliability under thermal cycling. The data show that these devices exhibit only modest change after the first 20 cycles, followed by stable behavior for up to 60 cycles. These results are shown in Figs. S9 and S10.

Stability – Stability is interpreted to refer to the response of devices to repeated electrical cycling and test. To explore this issue, we cycled the Si, GaN and SWNT devices up to 100 times. We observed changes in properties at the ~10% level, or less. These results are shown in Fig. S11.

Dispersion – We interpret dispersion to mean variations in device properties on a given substrate as well as between different substrates. The data appear in Figs. S12-15. We also explored the nature of defects that can appear in devices (due to processing, as opposed to printing, the latter of which is addressed in Fig. S3), which are summarized in Figs. S13-S15.
Figure S1. Image of the automated stage for transfer-printing.
Figure S2. (A) Optical micrographs of a two layer printed structure consisting of interconnected Si ribbons. The arrow indicates the shift between two layers, achieved by a rotation between printing steps. The left frame shows a schematic illustration of the structure. (B) Vector diagrams and a histogram plot of misalignment between the positions of particular features of printed-interconnected matrices of Si ribbons in a two layer stack with the size of 7.44 x 6.8 mm. The left vector diagram shows distortion after subtraction of the rotation between the layers. The middle diagram shows distortion after translational and rotational misalignments are subtracted. The right plot shows a histogram of the magnitudes of the distortion as defined in the middle frame. The median distortion is less than 0.5 μm.
Figure S3. (A) Optical images of the Si, GaN, GaAs and SWNT structures printed onto plastic substrates. The images highlight (red squares) the defects that can occur in the GaN and GaAs cases. (B) Transfer efficiencies from source to target substrates, as determined by optical and electron microscopy. The non-ideal printing yields of the GaN and GaAs structures result, in part, from their relatively large thicknesses and widths, respectively.

<table>
<thead>
<tr>
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<th>Yield for printing onto plastic substrates (%)</th>
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<tr>
<td>Si</td>
<td>99</td>
</tr>
<tr>
<td>SWNT</td>
<td>99</td>
</tr>
<tr>
<td>GaN</td>
<td>87.2</td>
</tr>
<tr>
<td>GaAs</td>
<td>95.5</td>
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Figure S4. (A) Optical micrographs of three dimensional, heterogeneously integrated arrays of Si MOSFETs and GaN HEMTs on a polyimide substrate. The right inset shows a cross sectional schematic view. The electrodes (gold), SiO₂ (PEO; purple), Si (light blue: undoped; dark blue: doped), GaN (dark green: ohmic contacts; light green: channel), polyimide (PI; brown) and polyurethane (PU; tan) are all shown. (B) Current-voltage characteristics of a typical Si MOSFET (channel length and width of 14 µm and 200 µm, respectively) and a GaN HEMT with (gate length and channel width 5 µm and 200 µm, respectively). The data for the Si and GaN in the left frames were measured at \( V_{dd} = 0.1V \) and \( V_{dd} = 2V \), respectively.
Figure S5. (A) Optical micrographs of three dimensional, heterogeneously integrated arrays of Si MOSFETs and SWNT TFTs on a polyimide substrate. The right inset shows a cross sectional schematic view. The electrodes (gold), SiO$_2$ (PEO; purple), Si (light blue: undoped; dark blue: doped), SWNTs (grey), polyimide (PI; brown) and cured polyimide (tan) are all shown. (B) Current-voltage characteristics of a typical SWNT TFT (channel length and width of 75 µm and 200 µm, respectively) and a typical Si MOSFET (gate length and channel width 19 µm and 200 µm, respectively). The data for the SWNT and Si in the left frames were measured at $V_{dd} = -0.5$ V and $V_{dd} = 0.1$ V, respectively.
Figure S6. (A) Schematic structure of the cross section of SWNT-Si CMOS inverter built on a silicon wafer substrate. (B) Transfer and I-V characteristics of Si and SWNT transistor forming CMOS inverter. (C) Calculated transfer characteristics of inverter and I-V characteristics of Si and SWNT transistor.
Figure S7. (A) Schematic structure of the cross section and circuit schematic of GaAs MSM-Si TFT IR detector built on a polyimide substrate. (B) Current-Voltage characteristic of GaAs MSM IR detector (L:10 µm, W=100 µm) and transfer and I-V characteristics of Si TFT (L = 9 µm, W = 200 µm) with a 3V supply. (C) Calculated I-V characteristic of GaAs MSM (channel length and width of 10 µm and 100 µm, respectively) and I-V response of a GaAs MSM integrated with a Si MOSFET (channel length and width of 9 µm and 100 µm, respectively) with a 3V supply.
Figure S8. Bending fatigue testing of 3 layer stacks of Si, GaN and SWNT transistors. (A) Images of the automated mechanical stages used to bend the system. (B) Normalized transconductances \( \frac{g_m}{g_{0m}} \) of devices in each layer after bending (to 3.7 mm radius) and unbending (to a flat state) the devices several thousand times. (black squares: Si MOSFETs; red circles: SWNT TFTs; green triangles: GaN HEMTs; blue triangles: Si MOSFETs with interlayer electrical via interconnects).
Figure S9. Thermal cycling tests (from 25 °C to 90 °C and back, over the course of 10 hours) on a substrate with a two layer stack of Si MOSFETs. (A) Transfer characteristics of Si MOSFETs on the top and on the bottom layer (channel length = 9 µm, channel width = 200 µm. $V_{dd} = 0.1$ V) for different numbers of thermal cycles. (B) The left plot shows a time diagram of the heating and cooling. The right tables show electrical properties evaluated at various stages of the test.

<table>
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<tr>
<th>Layer</th>
<th>$V_{th}$ (V)</th>
<th>Mobility ($\mu$) (cm²/Vs)</th>
<th>Subthreshold Slope (S) (mV/decade)</th>
<th>On/Off Ratio</th>
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<tr>
<td>Top Layer</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Before</td>
<td>-0.40</td>
<td>520</td>
<td>440</td>
<td>$6 \times 10^6$</td>
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<tr>
<td>20 cycles</td>
<td>-0.45</td>
<td>460</td>
<td>430</td>
<td>$6 \times 10^6$</td>
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<tr>
<td>60 cycles</td>
<td>-0.35</td>
<td>480</td>
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<tr>
<td>Bottom Layer</td>
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<td></td>
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<tr>
<td>Before</td>
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<td>527</td>
<td>394</td>
<td>$1 \times 10^6$</td>
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<tr>
<td>20 cycles</td>
<td>-0.86</td>
<td>433</td>
<td>379</td>
<td>$1 \times 10^6$</td>
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<tr>
<td>60 cycles</td>
<td>-0.82</td>
<td>464</td>
<td>379</td>
<td>$4 \times 10^6$</td>
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</table>
Figure S10. Thermal cycling tests (from 25 °C to 90 °C and back, over the course of 10 hours) on Si MOSFETs with interlayer electrical via interconnects. (A) Optical image and schematic illustration of the Si MOSFETs with interconnect metal lines. (B) Transfer curves and table of electrical properties of devices before and after cycling.
Figure S11. Electrical cycling tests on (A) Si MOSFETs (channel length = 9 µm, channel width = 200 µm, $V_{dd} = 0.1$ V). (B) SWNT TFTs (channel length = 50 µm, channel width = 200 µm, $V_{dd} = -0.5$ V). (C) GaN HEMTs (Gate length, channel width and gate width are 20 µm, 170 µm and 5 µm, respectively. $V_{dd} = 2$ V).
Figure S12. (A) Cross sectional schematic illustration of three dimensional, heterogeneously integrated arrays of Si MOSFETs, SWNT TFTs and GaN HEMTs on a polyimide substrate. (B) Transfer characteristics, effective mobilities and on/off ratios for several of the Si MOSFETs (channel width = 200 µm, black line: channel length = 9 µm, red: 14 µm, green:19 µm, blue: 24 µm), (C) the SWNT TFTs (channel width = 200 µm, black line: channel length = 25 µm, red: 50 µm, green:75 µm, blue: 100 µm) and (D) transfer characteristics, transconductances and on/off ratios for GaN HEMTs (channel lengths, widths and gate widths of 20 µm, 5 µm and 200 µm, respectively)
Figure S13. (A) Histograms of threshold voltages, on/off ratio and mobility of typical Si MOSFETs fabricated on eleven different substrates (channel length = 9 µm, channel width = 200 µm. $V_{dd} = 0.1$ V). (B) Optical images showing an example of device failure associated with a hairline crack formed in the silicon during processing.
Figure S14. (A) Histograms of threshold voltages, on/off ratio and mobility of typical SWNT TFTs fabricated on five different substrates (channel length = 50 µm, channel width = 200 µm. $V_{dd} = -0.5$ V). (B) Optical images showing an example of device failure by a defect associated with the photolithographic pattern of the source metal.
Figure S15. (A) Histograms of threshold voltages, on/off ratio and mobility typical GaN HEMTs fabricated on five different substrates (Devices with perfect ribbons were chose selectively. Gate length, channel width and gate width are 20 µm, 170 µm and 5 µm, respectively. $V_{dd} = 2$ V) (B) Optical images showing an example of device failure associated with a missing GaN bar.