

Reliable Memristive Switching Memory Devices Enabled by Densely Packed Silver Nanocone Arrays as Electric-Field Concentrators

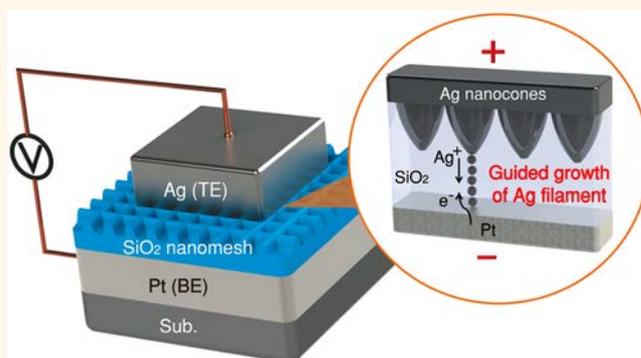
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S Supporting Information

ABSTRACT: Memristor devices based on electrochemical metallization operate through electrochemical formation/dissolution of nanoscale metallic filaments, and they are considered a promising future nonvolatile memory because of their outstanding characteristics over conventional charge-based memories. However, nanoscale conductive paths or filaments precipitated from the redox process of metallic elements are randomly formed inside oxides, resulting in unexpected and stochastic memristive switching parameters including the operating voltage and the resistance state. Here, we present the guided formation of conductive filaments in Ag nanocone/SiO₂ nanomesh/Pt memristors fabricated by high-resolution nanotransfer printing. Consequently, the uniformity of the memristive switching behavior is significantly improved by the existence of electric-field concentrator arrays consisting of Ag nanocones embedded in SiO₂ nanomesh structures. This selective and controlled filament growth was experimentally supported by analyzing simultaneously the surface morphology and current-mapping results using conductive atomic force microscopy. Moreover, stable multilevel switching operations with four discrete conduction states were achieved by the nanopatterned memristor device, demonstrating its potential in high-density nanoscale memory devices.

KEYWORDS: solvent-assisted nanotransfer printing, nanomesh structure, memristive switching, conductive filament, multilevel cell



The memristive switching phenomenon of metal–insulator–metal (MIM) structures can be exploited in next-generation memory devices,^{1–7} reconfigurable logic circuits,^{8–10} and neuromorphic^{11–14} applications due to its nonvolatile memory characteristics, fast response, simple structure, high density, and low power consumption. Among the various types of memristive switching behaviors, the electrochemical metallization (ECM) mechanism is based on the growth and dissolution of nanoscale conductive filaments (CFs) into solid electrolyte through the redox process as a result of metal/electrolyte charge transfer and the migration of metallic cations (e.g., Ag or Cu).^{15–23} These ECM memories have attracted much attention as a promising candidate for next-generation nonvolatile memories because of their outstanding properties, including a small operating current, large on/off resistance ratio ($R_{\text{on}}/R_{\text{off}}$), good reliability, and applicability to multilevel cell (MLC) storage.^{17,18,24–28} However, in filament-

type ECM memories with memristive switching, nanoscale CFs grown at random locations could lead to unexpected switching properties or even failures which are usually caused by large fluctuations in the operating voltages and resistance states.^{3,6,29–31} This nonuniform and inconsistent resistive switching performance adversely affects MLC applications, thereby hindering high-density data storage. To resolve this issue of random formation of CFs, various methods have been proposed including impurity doping,^{32,33} insertion of an interfacial layer^{34,35} or metal nanoparticles,^{29,30,36} and customized memory structures.^{37,38} We also previously suggested the insertion of nanostructures as a solution to control the formation of CFs by exploiting uniformly arrayed sub-20 nm insulating

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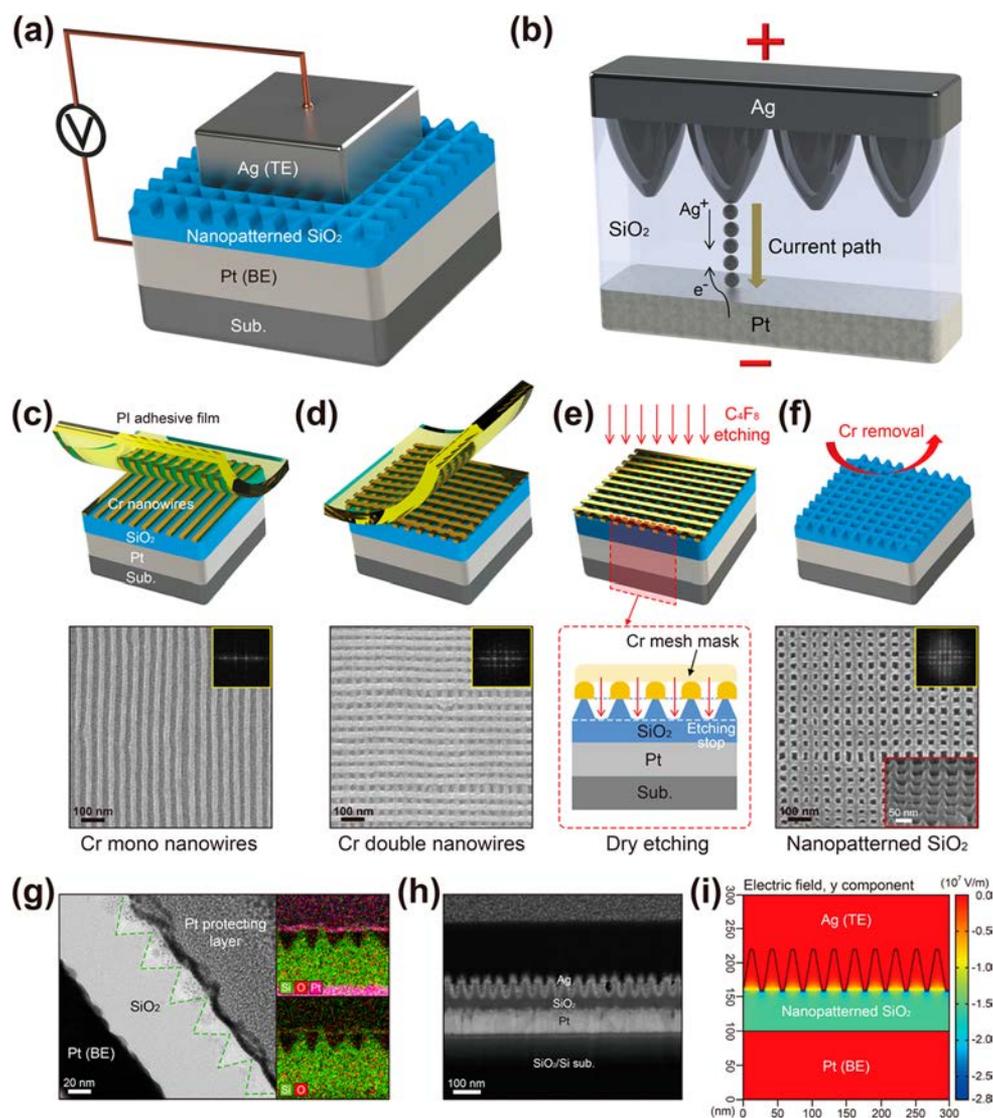


Figure 1. (a) Schematic of the Ag nanocones/nanopatterned SiO₂/Pt memristor device. (b) Memristor switching mechanism explaining the Ag filament growth at the electric-field-enhanced sites of the SiO₂ films. (c–f) Schematics and SEM images of the fabrication steps for the SiO₂ layer patterned through the Cr nanomesh mask obtained by using the S-nTP method with BCP templates. (c) First printing of the Cr nanowires onto the SiO₂ films. (d) Second printing of the Cr nanowires perpendicular to the underlying nanowires. The width/pitch of the Cr mesh mask were 25 nm/50 nm, respectively. (e) Dry etching of the SiO₂ films with C₄F₈ gas. (f) Removal of the Cr mesh mask using a wet etchant. The inset images of c, d, and f show the fast Fourier transform patterns of the SEM images. (g) TEM and EDS elemental mapping images of the nanopatterned SiO₂ layer. (h) SEM image of the fabricated Ag nanocones/nanopatterned SiO₂/Pt memristor device. (i) FEM simulation of the device for electric-field distributions in nanopatterned SiO₂ films.

SiO_x nanodots derived from self-assembled Si-containing block copolymers (BCPs) in unipolar NiO-based resistive memories.³¹ Nevertheless, more effective and scalable nanoscale methods are still required to achieve sufficient performance enhancements and reliable resistive switching behaviors in ECM memories.

In this study, we first demonstrate that the patterning of a SiO₂ solid electrolyte layer into a sub-10 nm nanomesh structure *via* the solvent-assisted nanotransfer printing (S-nTP) can selectively guide the positions of nanoscale Ag filaments in a memristor device. The SiO₂ in the ECM memory of the Ag/SiO₂/Pt structure was uniformly patterned with the S-nTP method based on self-assembled BCP templates and a series of subsequent anisotropic plasma etching and Ag deposition processes. This successfully provides well-defined interdigitated nanostructures composed of Ag nanocones and SiO₂ nanomeshes, in which the electric field is highly concentrated between

the tip end of the Ag nanocones and SiO₂. This locally electric (*E*)-field-enhanced Ag/SiO₂/Pt memristor device, which is also supported by finite element method (FEM) simulations, substantially improved the memristive switching parameters, including the operating voltages and resistance states. Simultaneous morphology and current scanning with a conductive atomic force microscope (C-AFM) system also confirmed that the Ag filaments are mostly grown in the *E*-field-enhanced nanoscale valleys. Finally, our nanostructured memristor device, which achieved highly selective and controlled memristive switching, also showed stable and reproducible MLC operations with four discrete levels (a maximum of six levels).

RESULTS AND DISCUSSION

Nanomesh-Patterned Memristor Devices Using S-nTP Method. The nanostructured Ag top electrode (TE)/nano-

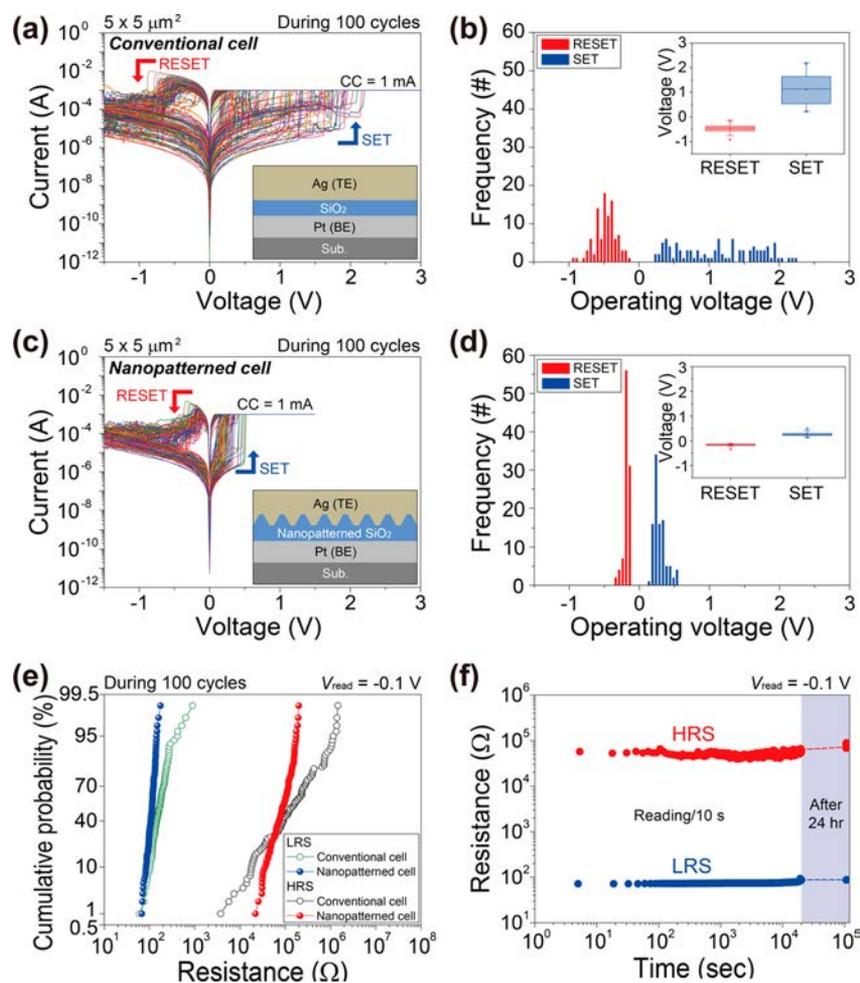


Figure 2. (a) I – V curves and (b) histograms of the reset/set operating voltage in the conventional Ag/SiO₂/Pt memristor unit cell during 100 cycles. (c) I – V curves and (d) histograms of the reset/set operating voltage in the Ag nanocones/nanopatterned SiO₂/Pt memristor unit cell for 100 cycles. The insets of b and d show the statistical charts of the operating voltage. (e) Cumulative probability of high-resistance state (HRS)/low-resistance state (LRS) values for the conventional and nanopatterned memristor unit cell during 100 cycles. (f) Time retention test result of the nanopatterned memristor cell up to 10⁵ s. The reading voltage for all resistance measurements was –0.1 V.

patterned SiO₂/Pt bottom electrode (BE) memristor device for guiding the Ag filaments is shown in Figure 1a. This specific nanopatterned structure was designed with E -field-concentrated regions to provide a local nanoscale supplier of Ag ions (Figure 1b). When a positive voltage is applied to the Ag TE, both oxidized Ag ions and electrons migrate to the nanopatterned SiO₂ solid electrolyte in the opposite direction followed by the reduction and precipitation of the Ag nanofilaments.^{3,15,20,21,26} The process steps for the nanopatterned solid electrolyte layer are based on the S-nTP technique, which is a very simple and cost-effective technique with high resolution (Figure 1c–f),³⁹ compared to conventional nanotransfer printing (nTP) using an elastomeric mold.^{40,41} This s-nTP method can easily produce well-defined two- and three-dimensional nanostructures in the deep-nanoscale regime (sub-10 nm resolution) with high transfer printing yield due to the adoption of a disposable polymer thin film replica and distinct transfer mechanism based on solvent-assisted adhesion switching. A nanograted master template was prepared with poly(styrene-*b*-dimethylsiloxane) (PS-*b*-PDMS) BCP (MW = 48 kg mol⁻¹) self-assembly. Poly(methyl methacrylate) (PMMA) was then spin-coated onto the master template, and the coated PMMA replica films were peeled off using a polyimide (PI) adhesive film. Cr metal, which was

specifically chosen for the selective etching of the SiO₂ films, was deposited on the replica at a 75° angle from the substrate surface normal. The angled deposition technique based on an e-beam evaporator is very important to fabricate well-defined Cr nanowires. In the case of general thin film deposition, a continuous and conformal Cr thin film is formed on the polymer replica, while an angled deposition technique forms discrete Cr nanowires on the recessed regions from the polymer replica due to the shadowing effect (Figure S1d, Supporting Information). The Cr nanowires/PMMA/PI films were exposed to a mixed solvent vapor of acetone and heptane to reduce the adhesion between the Cr nanowires and thin film replica.³⁹ The fabricated Cr nanowires on the replica films were directly transferred to the SiO₂ (120 nm)/Pt (100 nm) deposited substrate (Figure 1c). The width and pitch of the transferred Cr mono-nanowires were 25 and 50 nm, respectively, as shown in the scanning electron microscopy (SEM) image of Figure 1c. Additional Cr nanowire arrays with perpendicular alignment with the underlying nanowires were subsequently transferred by the same transfer process steps, resulting in the Cr mesh nanostructures (Figure 1d). It should be noted that the present S-nTP method is more advanced than the previous S-nTP technique proposed by our group.³⁹ The process steps were simplified by reducing the

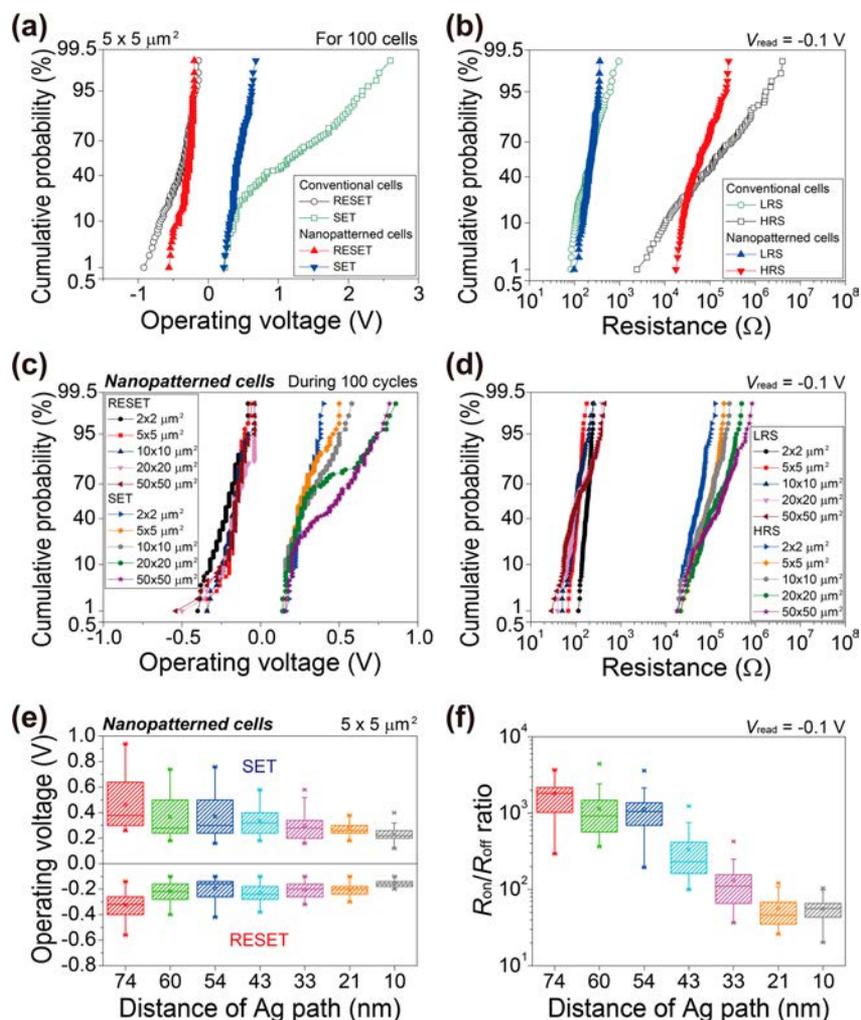


Figure 3. Cumulative probability graphs of (a) operating voltages and (b) resistance states in 100 different conventional/nanopatterned memristor cells with a $5 \times 5 \mu\text{m}^2$ active area. Cumulative probability graphs of (c) operating voltages and (d) resistance states of nanopatterned memristor cells with various electrode areas from 2×2 to $50 \times 50 \mu\text{m}^2$ during 100 cycles. (e) Operating voltage distributions and (f) $R_{\text{on}}/R_{\text{off}}$ ratio depending on the thickness of SiO_2 solid electrolyte (filament path) between Ag nanocones and the Pt BE.

number of transfer printing, resulting in the increased yield of nanopattern transfer. The details of the fabrication process for the metal mesh nanostructures are described in the [Experimental Section](#) and Figure S1 of the [Supporting Information](#). The SiO_2 films were then patterned using anisotropic dry etching with a 60 nm thick residual layer as the Ag filament growth path (Figure 1e). Plasma etching with C_4F_8 gas provides high selectivity (etch rate) between the SiO_2 films and Cr nanowires, in which the Cr mesh mask acts as an excellent etching mask. Finally, the Cr mesh mask was removed by wet etchant. Completed nanomesh-directed patterned SiO_2 films are shown in Figure 1f. Additional AFM scanning images, corresponding SEM images, and low-magnification SEM images confirmed that the nanoprinting methods of this study attained very uniform and well-aligned nanostructures (Figures S2 and S3, [Supporting Information](#)). The average width of square holes on the nanomesh-directed patterned SiO_2 films was 26.7 nm, which was estimated from a top-view SEM image shown in Figure 1f (Figure S4, [Supporting Information](#)). As shown in the cross-sectional transmission electron microscopy (TEM) image and energy-dispersive spectrometer (EDS) elemental mapping results of Figure 1g, anisotropic plasma etching of SiO_2 formed sawtooth-shaped nanostructures.

For the formation of the ECM memristor device composed of sharp Ag nanocones and SiO_2 nanomesh structures, Ag TE (20 nm) was uniformly deposited on the nanopatterned SiO_2 films with a sputtering system (cross-sectional SEM image in Figure 1h). The active device area of the memristor device with a cross-point structure, which was defined by the conventional optical lithography process, is $5 \times 5 \mu\text{m}^2$. To investigate the mechanism of the nanomesh-patterned memristor, the electric-field distributions were analyzed by FEM-based simulation. Figure 1i shows that the electric fields are concentrated on the nanopatterned valleys, which correspond to the shortest path between the Ag TE and the Pt BE. These electric-field-modified nanopatterned structures can guide the formation of Ag CFs at the designated regions, enabling reproducible and repeatable migration or drift of Ag ions into the SiO_2 solid electrolyte.

Electrical Performance. The electrical characteristics of the fabricated memristor devices were measured with a semiconductor analyzer using direct current (dc) sweeping mode. The voltage was applied to the Ag TE, while the Pt BE was grounded. The compliance current (cc) was set up as 1 mA to prevent thermal-induced breakdown of the devices in the positive bias voltage region.^{42,43} To compare the resistive switching behaviors, a conventional memristor device was

prepared (active area of $5 \times 5 \mu\text{m}^2$) whose structure was a Ag TE/flat SiO_2 film (60 nm)/Pt BE without any nanomesh structures. The electrical measurement results of the conventional memristor cell during 100 cycles are shown in Figure 2a,b. The current–voltage (I – V) curves in Figure 2a indicate a typical bipolar switching behavior for the conventional memristor cells; that is, reset/set switching occurs at the opposite bias polarities. The histograms and statistical charts in Figure 2b show the operating voltage distributions obtained from the I – V curves. The reset and set voltage ranges were -0.14 to -0.92 V and 0.22 to 2.2 V, respectively. These widespread operating voltage ranges of the conventional cells originate from random Ag filament formations in the SiO_2 solid electrolyte. In contrast, reproducibility and repeatability of the operating voltages in the nanomesh-directed patterned memristor cell (with an active area of $5 \times 5 \mu\text{m}^2$) was remarkably improved, as seen in Figure 2c,d. The reset and set voltage ranges were -0.12 to -0.34 V and 0.14 to 0.52 V, respectively, which were much narrower than those of the conventional cells. For further quantitative analysis of the memristive switching voltage variations, the standard deviation (SD) of the switching voltages was also calculated. The average/SD operating voltages of the conventional cells were -0.466 V/ 0.148 V (reset) and 1.113 V/ 0.574 V (set). On the other hand, the corresponding values of the nanopatterned cells were -0.160 V/ 0.045 V (reset) and 0.273 V/ 0.088 V (set). In other words, the SD of the reset and set voltages were reduced by 69.6 and 84.7%, respectively, by the nanomesh patterning.

These improved memristive behaviors can be explained by the selective and reproducible growth of the Ag CFs through the nanopatterned SiO_2 layer shown in the schematic of Figure 1b. In the case of the ECM mechanism, both growth and dissolution of the Ag CFs are induced from the local electric fields concentrated by defects or impurities in the solid electrolyte.^{3,15} While it is difficult to manipulate these intrinsic properties of the materials with conventional approaches, the nanopatterning strategies proposed in this study successfully modified the electric fields. As a result, the repeatability and reliability of both the reset and set voltages were enhanced significantly. In addition to the operating voltages, the resistance values of the memristor cells (read voltage = -0.1 V) during 100 cycles are shown in Figure 2e. For the nanopatterned cells, variations in both the resistance values of the high-resistance state (HRS) and low-resistance state (LRS) significantly decreased when compared with those of the conventional cells. Generally, the LRS value depends on the number and/or the size of the metallic CFs, while the HRS value originates from the length of ruptured filaments, that is, the tunneling gap distance.^{6,20,22,31,44} Thus, it is necessary to manage the reproducible and selective activation/dissolution of Ag filaments to reduce fluctuations in the HRS and LRS values. The time retention property of these uniform resistance states of the nanopatterned cells is shown in Figure 2f. The HRS/LRS ratio of the devices was maintained for longer than 10^5 s at room temperature without any distinct degradation.

Figure 3a,b shows the cumulative probability distribution of the memristor switching voltages and the resistance states in 100 conventional/nanopatterned cells with an electrode area of $5 \times 5 \mu\text{m}^2$. For the nanopatterned cells, both the reset/set operating voltages and the resistance states (HRS/LRS) show narrow distributions for the 100 randomly chosen different memristor cells, which implies that the S-nTP process enables uniform nanostructure formation in the entire sample area. This can be understood based on the electrical characteristics shown in Figure 2a–d, which shows that the nanopatterning successfully

enhanced the uniformity of the resistive switching voltages and the resistance states in a memristor cell area of $5 \times 5 \mu\text{m}^2$. To further investigate the influence of the electrode area on the electrical performance of the memristor cells, devices with different active areas ranging from 4 to $2500 \mu\text{m}^2$ (2×2 , 5×5 , 10×10 , 20×20 , and $50 \times 50 \mu\text{m}^2$) were measured for 100 cycles (Figure S5, Supporting Information). All of the cells showed remarkable uniformity enhancements of the reset/set voltages and the HRS/LRS levels, which was confirmed by a comparison between the cumulative probability distributions of Figure 3c,d (nanopatterned cell) and those of Figure S6 in the Supporting Information (conventional cell). According to these data, the uniformity of the operating voltages and the resistance states in the nanopatterned cells tends to improve with a reduction in the electrode area. In particular, this dependency is more dominant in the set voltage because the number of filament formation positions decreases with the reduction in cell area. In the micrometer-scaled cell size, the influence of the nanopatterned solid electrolyte layer becomes significant, although the electrode area is the main factor for the reproducibility of the switching voltages. This indicates that local electric-field management by the nanopatterning process can effectively control the formation of nanoscale Ag CFs in ECM memristor devices. In fact, our memristor device size (minimum of $2 \times 2 \mu\text{m}^2$) is relatively large to claim the scalability aspect of nanopatterned devices. However, it is clear that memristor switching of the sub-100 nm device (only four electric concentrators in the 26 nm patterning process) would show characteristics more uniform and reliable than those of $2 \times 2 \mu\text{m}^2$ memristor cells. We already showed uniformity improvement depending on device size in Figure 3c,d. Thus, we believe that reliability and uniformity of a smaller-sized device employing our approaches can be improved.

To additionally study the scaling dependency of the Ag filament path, we performed the control test regarding the thickness dependence of the SiO_2 layer as a filament path between Ag nanocones and the Pt BE, as shown in Figure 3e,f. As a result, both reset and set voltages during repeated memristive switching were proportionally decreased with a reduction of the Ag CF path distance in the nanopatterned cells (Figure 3e). In addition, when the distance of the filament path was smaller, the uniformity of the operating voltages was more improved. These tendencies could be caused by a reduction of the thickness/number of initial Ag CFs grown into the thinner solid electrolyte. Although this memristor device shows outstanding properties of low voltage and high uniformity, thinning of the filament path leads to a reduction of the $R_{\text{on}}/R_{\text{off}}$ ratio, as shown in Figure 3f. Especially, this reduction of the resistance ratio is contributed by the lower HRS. The smaller reset voltage induces less dissolution of Ag filaments, resulting in the reduction of the HRS. The leakage current generated from a thin SiO_2 layer also may cause the reduction of the HRS. This trade-off relation between operating voltages and the $R_{\text{on}}/R_{\text{off}}$ ratio is important because these switching parameters could affect the MLC operation of the memristor device.

Furthermore, sub-10 nm nanopatterned SiO_2 films were fabricated with the Cr nanomesh mask using PS-*b*-PDMS BCPs with an even smaller molecular weight ($\text{MW} = 36 \text{ kg mol}^{-1}$). The average width of the square holes on the SiO_2 films was 9.8 nm, which was estimated from a top-view SEM image in Figure S7a in the Supporting Information. The Ag/sub-10 nm nanopatterned SiO_2 /Pt memristor device was fabricated with the same process steps except for the decreased pattern size of the SiO_2 films, whose electrical characteristics are shown in Figure S7c,d in the

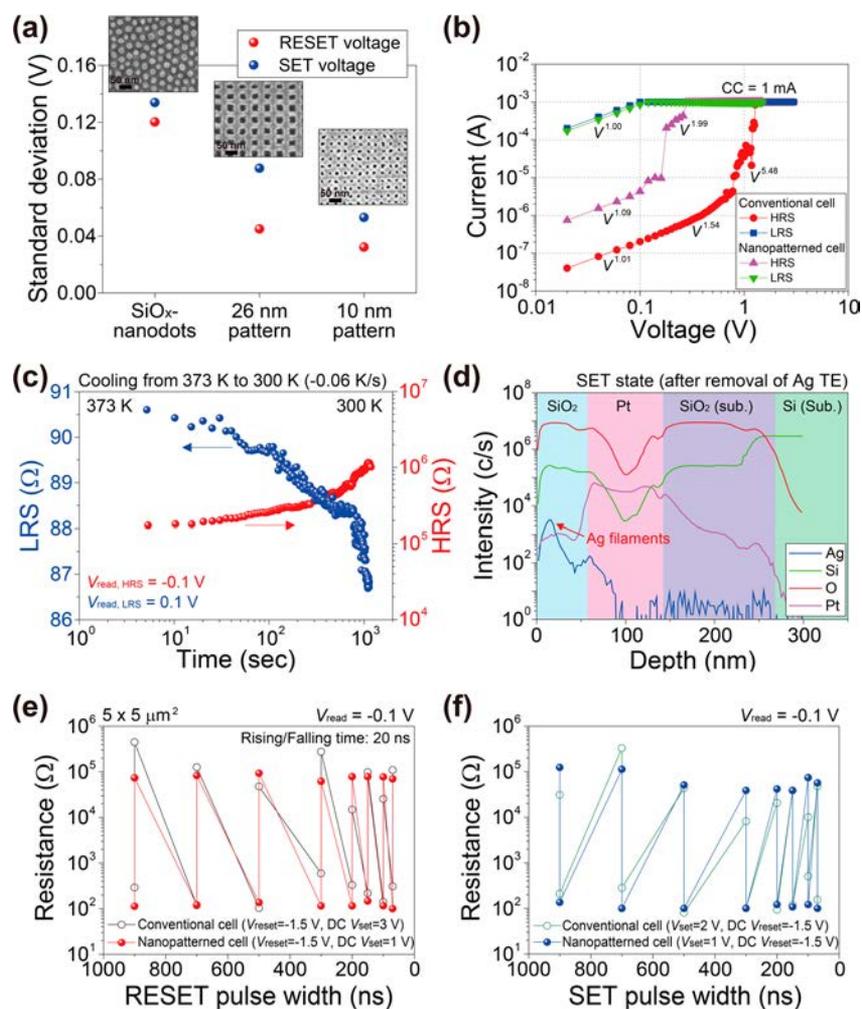


Figure 4. (a) Standard deviation of the operating voltage in memristor devices with 20 nm diameter self-assembled SiO_x nanodots, 26 nm nanopatterned SiO₂, and 10 nm nanopatterned SiO₂. The width/pitch of the Cr mesh mask for the 10 nm nanopattern were 13 nm/23 nm, respectively. (b) Log–log I – V plots from the set process region of the conventional and nanopatterned cells. (c) Resistance change depending on temperature (cooling from 373 to 300 K) of the nanopatterned memristor cell. The read voltage for HRS/LRS was -0.1 V/ 0.1 V, respectively. (d) Secondary ion mass spectrometry (SIMS) analysis from the nanopatterned cell after the set process. The Ag TE was completely removed before the SIMS measurement. Response time of (e) reset process and (f) set process depending on the switching pulse width.

Supporting Information. As a result, the SD of the reset/set voltage in the sub-10 nm nanopatterned cell was 0.038 V/0.053 V, respectively, which was smaller than those (0.045 V/0.088 V) of the 26 nm nanopatterned memristor cells shown in Figure 4a. In other words, the creation of smaller nanostructures in memristor devices is more beneficial, ensuring the uniformity and reproducibility of the memristor switching because the size of electric-field-concentrated areas is extremely reduced. This result suggests that the proposed approach can be applicable to highly integrated devices with sub-20 nm active areas.

For an additional comparison, a Ag/self-assembled SiO_x nanodots/SiO₂/Pt memristor device was fabricated and measured under the same conditions. To form hexagonally aligned SiO_x nanodots on SiO₂ films, a PS-*b*-PDMS BCP was spin-coated onto the prepared sample followed by the vacuum-assisted thermal annealing for the self-assembly at 150 °C. CF₄ and O₂ plasma treatments remove the PS matrix and convert the PDMS spheres into SiO_x nanodots. The detailed process of BCP self-assembled SiO_x nanodots is described in the [Experimental Section](#). The average diameter and height of the silica nanodots were 20 and 10 nm, respectively (Figure S8a,b, [Supporting](#)

[Information](#)).⁴⁵ Our group previously reported that self-assembled SiO_x nanodots using Si-containing PS-*b*-PDMS BCPs substantially improved the uniformity of the resistive switching parameters in NiO-based unipolar resistive memories based on CF formation/rupture by oxygen vacancy migration.³¹ The metallic Ni filaments were grown and ruptured at the regions between incorporated insulating silica nanodots because of the enhanced electric field and modification of heat distributions. In the case of ECM bipolar memories, the uniformity of the switching voltages was also improved (Figure S8c,d, [Supporting Information](#)). However, the SD of the reset and set voltages of Ag/20 nm SiO_x nanodots/SiO₂/Pt cell was 0.120 and 0.134 V, respectively, which is larger than those of the nanopatterned cells shown in Figure 4a. There could be two reasons for the increase in the SD values: (1) electric-field-enhanced areas are much smaller in the S-nTP-directed nanopatterned cells, in which Ag filaments are formed in a smaller number of positions, and (2) the aspect ratio of the nanomesh-directed SiO₂ pattern is larger than that of the self-assembled SiO_x nanodots, which yields more definite electric-field separation between each nanopattern. Therefore, the proposed S-nTP-based approach is more

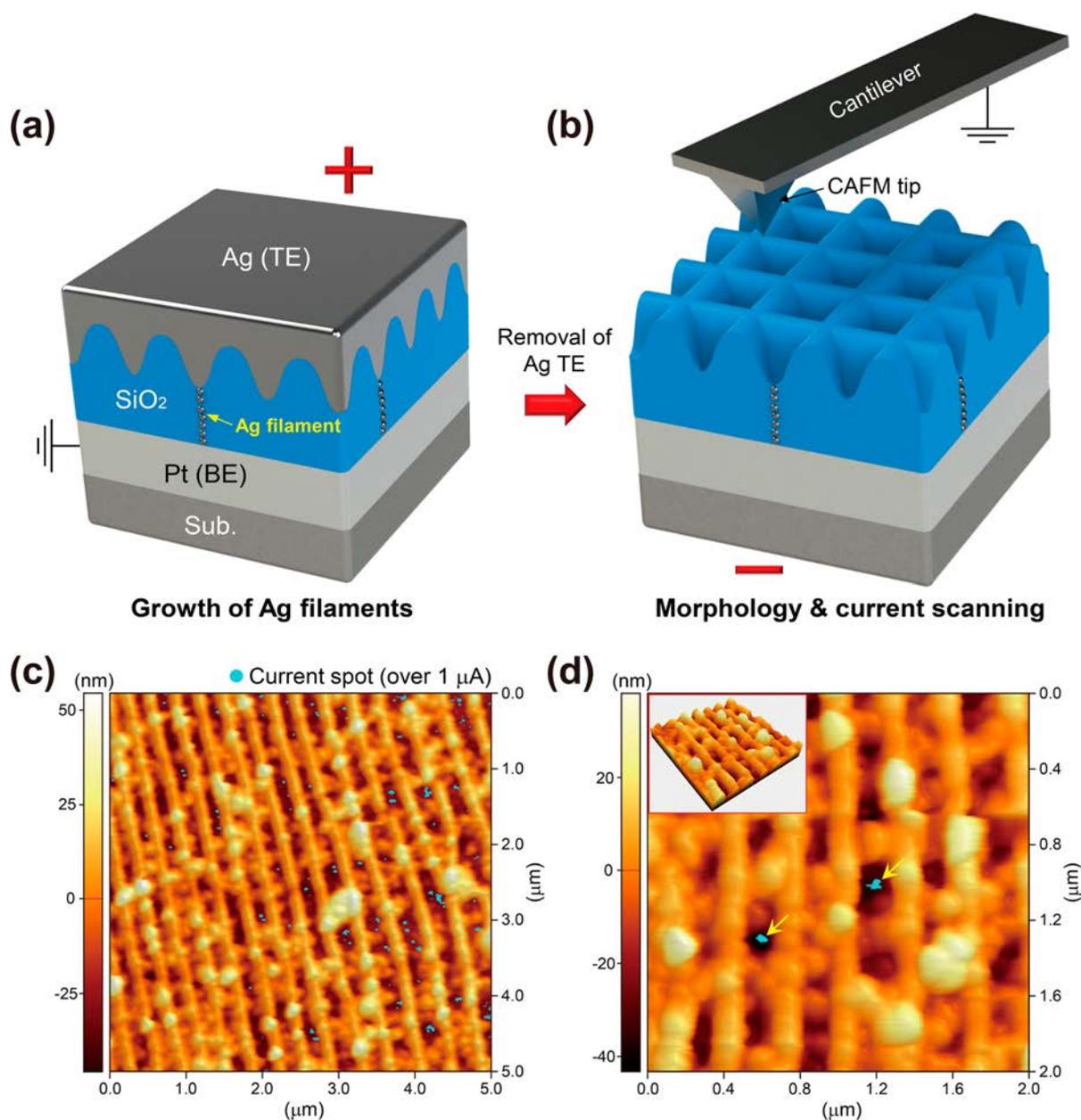


Figure 5. (a,b) Process steps for position detection of the Ag filaments grown in the nanopatterned SiO₂. The width/pitch of Cr mesh mask used for C-AFM analyses were 50 nm/200 nm, respectively. (a) Formation of the Ag filaments by applying the positive voltage to the Ag TE. (b) Simultaneous morphology and current scanning using the C-AFM system after removal of the Ag TE. The sample voltage bias was -1.0 V, and the C-AFM tip was grounded. C-AFM results from (c) $5 \times 5 \mu\text{m}^2$ and (d) $2 \times 2 \mu\text{m}^2$ scan areas. The yellow arrows of d indicate the Ag filament spots, and the inset shows the tilted 3D topography scan image.

preferable for the formation of Ag CFs controlled by the effective electric-field concentration.

ECM Mechanism Analysis. Although it was previously shown that resistive switching in the Ag/SiO₂/Pt structure was based on the ECM mechanism, we need to confirm the existence of Ag CFs in the SiO₂ solid electrolyte. Figure 4b shows the I - V curves replotted in log-log scale in the positive voltage region. The I - V characteristic of the LRS in both the conventional and nanopatterned cells follows a linear Ohmic conduction model, with a slope of 1.00 indicating that CFs of our Ag/SiO₂/Pt memristor act as metallic conductive paths.^{26,33} In the HRS, on the other hand, the I - V curve of two cells shows a nonlinear characteristic with increasing slopes for larger applied voltages, which agrees with the conduction model of an insulator.^{46,47}

Additional evidence of the ECM mechanism is the temperature dependency of the HRS/LRS shown in Figure 4c. The *in situ* measurement of the resistance states as a function of temperature was custom designed to apply the read voltage every 5 s with a cooling rate of -0.06 K/s (from 373 to 300 K). The reading voltage for HRS and LRS was set to -0.1 and 0.1 V, respectively, to prevent any unexpected switching behaviors. The LRS value slightly decreased with a reduction in temperature, implying that the high conductivity of our nanopatterned memristor cells resulted from the growth of the Ag metallic CFs.^{3,26,31} In contrast, the HRS value increased with a decrease in temperature, indicating the insulating or semiconducting behavior of the SiO₂ solid electrolyte.^{26,48} To provide direct detection of the Ag filaments, secondary ion mass spectrometry (SIMS) analyses

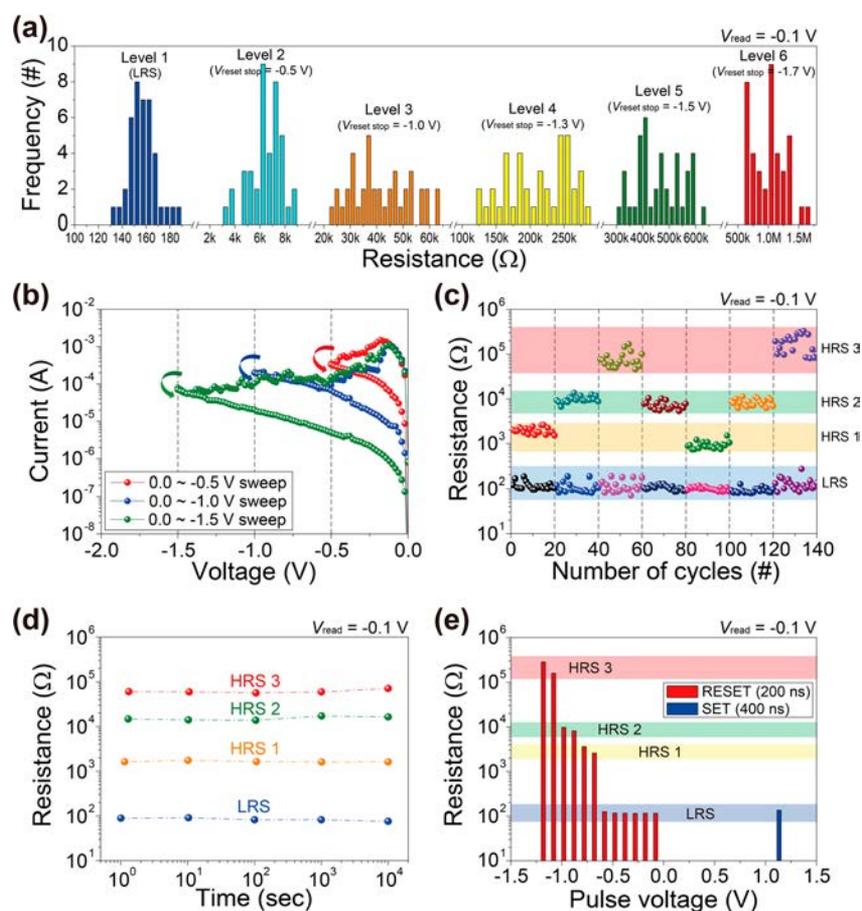


Figure 6. (a) Histogram of MLC occurrence frequency for the sub-10 nm patterned memristor cell depending on the reset stop voltages (six resistance levels). (b) I - V curves for MLC operations (reset process region). (c) Cycling endurance and (d) time retention measurement results from four-level resistance states. (e) Pulse operation results for realizing MLC applications. The pulse width for the reset/set processes was 200 ns/400 ns, respectively.

were also done after removal of the Ag TE in the set state of the memristor cells (Figure 4d). The Ag peak was detected in the SiO_2 active layer, which is distinguished from the SIMS measurement results for the initial state shown in Figure S9 in the Supporting Information. These multiple lines of experimental evidence confirm that the resistive switching behavior in our memristor cells is based on the ECM mechanism.

Response Time Measurements. In order to evaluate the response time of our ECM memristor cells, the reset and set writing speed were measured as shown in Figure 4e,f, respectively. For the estimation of reset (set) pulse width, the following set (reset) process was applied by dc sweep voltage. For both patterned and nonpatterned memristor cells, the resistance values were changed over 2 orders by changing the pulse width from 900 to 70 ns, and the minimum pulse width (reset and set) was set by the specification range of our semiconductor analyzer. Yang *et al.* previously reported the ECM-based resistive memory consisting of conventional Ag/ZnO:Mn/Pt structure with fast writing speed of 5 ns.²⁶ We believe that our nanopatterning process did not significantly affect the response time of memristor devices. Nevertheless, the ECM-based memristor has an operation speed much higher than that of the charge-based flash memory, which is one of its outstanding advantages as next-generation nonvolatile memories.

C-AFM Scanning of the Ag Filaments. The nanomesh-patterned ECM memristor becomes reliable and reproducible

through the confinement of Ag CFs at specific positions, at which the electric field is highly concentrated. To visualize this phenomenon, C-AFM scanning was experimentally introduced in our devices. A C-AFM system is useful to simultaneously observe the size, position, and 3D structure of CFs in filament-type resistive memories.^{29,49,50} When the C-AFM system is in the contact mode, accurate mapping of sub-20 nm morphologies is difficult because the tip-end diameter of the Pt-coated AFM tip is 20 nm. Hence, a new Cr nanomesh mask with a 50 nm width and 200 nm pitch was prepared using master templates fabricated by the conventional photolithography process seen in the SEM images of Figure S10 in the Supporting Information. The SiO_2 solid electrolyte layer was patterned with a relatively wide Cr mesh mask followed by the same fabrication process steps for the memristor devices. Positive voltage was applied to the Ag TE using a semiconductor analyzer; the Ag CFs were then grown in the nanopatterned SiO_2 layer shown in Figure 5a. After the formation of the Ag filaments, the Ag TE was completely removed by wet-etchant solution. Morphologies and currents were simultaneously scanned using a Pt-coated C-AFM tip probed onto the nanopatterned SiO_2 surface (Figure 5b). To obtain a more clearly scanned image, the C-AFM cantilever was electrically grounded, while a negative voltage bias of -1.0 V was applied to the Pt BE. Figure 5c,d shows the overlapped scanned images of the morphology and current outputs in the 5×5 and $2 \times 2 \mu\text{m}^2$ scan areas, respectively. Each individual scanned image is shown in Figure S11 in the Supporting Information. The

output current spots mean highly conductive paths, which indicate the Ag CFs in our ECM memristor devices. All current spots higher than $1\ \mu\text{A}$ were detected at the lowest points (nanopatterned valleys) or the electric-field-concentrated regions, indicating that the Ag filaments were selectively grown at the junction points between the nanoholes in the SiO_2 and the tip ends of the Ag nanocones. These results of the simultaneous mapping of the morphologies and current provide direct evidence of the uniformity improvements in the ECM memristor switching parameters.

MLC Application. Cross-point-structured memristor devices are suitable for high scalability due to their simple structure and MLC applicability.^{3,6,7,38,43,44,51–53} Thus, it is important to analyze the MLC characteristics of the nanopatterned ECM memristor in this study. For MLC switching operations, the sub-10 nm patterned memristor cell was used because of its excellent switching uniformity. The MLC operations of our ECM memristor devices can be achieved by modulation of reset stop voltage or compliance current in the set process. When the partial reset voltage was applied to the device, discrete resistance states of six levels were established without any overlap, as shown in Figure 6a. Generally, a filament-type bipolar memristor device shows a gradual reset transition, which is related to a slow but continuous dissolution of CFs away from the electrode.^{53–55} We suggest that this gradual reset phenomenon by the applied voltage bias can be used to achieve multistep resistance states, which are attributed to the controlled changes of (i) the number of Ag filaments, (ii) the thickness of Ag filaments, and (iii) the tunneling gap between nanocrystals of Ag filaments.^{56,57} When higher reset voltage is applied to the device, a Ag filamentary path is completely ruptured with a sharp current drop. As this fully ruptured filament pathway can cause the significant resistance fluctuations, we did not use this high resistance level in MLC applications. Among the six levels, very stable and reproducible four multistep resistance levels (level 1, level 2, level 3, and level 5) were selected. Figure 6b shows the representative I - V curves with sweeping voltages in the negative voltage regions (reset process). After the set process, three reset sweeping voltages of -0.5 , -1.0 , and -1.5 V were applied to the device using the dc voltage mode, enabling three discrete HRSs and one LRS at a reading voltage of -0.1 V. Although this MLC switching is a main advantage of ECM memristors, it is difficult to implement due to its nonuniform and inconsistent switching parameters caused by random filament formation/rupture.^{6,31,33} The MLC cycling endurance test was done with four-level resistance states in our sub-10 nm patterned cell shown in Figure 6c. The four memory states (LRS, HRS1, HRS2, and HRS3) were successfully achieved with reproducible and stable resistance states in either the forward or reverse direction, showing the reliable recovery back to previous resistance levels. In the case of our conventional ECM memristor device, four-level MLC operations were also observed. However, the resistance levels did not revert to their initial resistance states during cycling endurance in both directions (Figure S12, Supporting Information). Therefore, we can emphasize that our nanopatterning process *via* S-nTP contributes to uniformity and reliability improvements of the MLC application. To examine the device stability, the retention property of each resistance level was measured for up to 10^4 s at room temperature. There was no apparent degradation observed in any of the resistance levels shown in Figure 6d. Moreover, MLC switching with a voltage pulse was also attempted (Figure 6e). The pulse width of the reset and set operation was set to 200 and 400 ns, respectively. In the case of the reset process, the pulse

amplitude for each resistance level was assigned as -0.6 to -0.7 V, -0.9 to -1.0 V, and -1.1 to -1.2 V for HRS1, HRS2, and HRS3, respectively. These MLC characteristics show that the nanopatterned memristor devices in this study are sufficient for high-density and scalable memory applications.

CONCLUSIONS

In summary, a hybrid architecture composed of Ag nanocone arrays and a SiO_2 nanomesh was developed to improve the switching uniformity of ECM-based memristor devices, achieving a markedly more reproducible and reliable operating voltage and resistance state compared to conventional devices. Our device structure was fabricated with the S-nTP nanopatterning process with excellent scalability and fine resolution to form a Cr nanomesh hard mask on the SiO_2 films, which are the solid electrolyte layer of the Ag/ SiO_2 /Pt ECM memristor cells. Various electrical characteristics and C-AFM analyses validated how the Ag nanostructures contained in the memristor cell can control the formation of nanoscale CFs inside SiO_2 . Furthermore, stable and repeatable MLC switching was confirmed especially in the sub-10 nm-scale patterned devices by showing clearly distinguishable four-level conduction states. We expect that this innovative nanoscale patterning approach can be used as a promising strategy for various high-density and high-performance memory applications in the future.

EXPERIMENTAL SECTION

Fabrication of Master Mold. PS-*b*-PDMS (MW = 36 kg mol⁻¹, SD36), PS-*b*-PDMS (MW = 48 kg mol⁻¹, SD48) BCPs, which form 13 and 20 nm wide lines, respectively, and a hydroxyl-terminated PDMS brush (MW = 5 kg mol⁻¹) were purchased from Polymer Source Inc. (Canada). The solutions of hydroxyl-terminated PDMS brush (1.5 wt %), SD36 (0.6 wt %), and SD48 (0.75 wt %) were prepared and used for self-assembled line/space patterns. For the directed self-assembly, surface-patterned Si substrates with a width of 1 μm and a period of 1.25 μm were treated with a PDMS brush at 200 °C using a vacuum oven. The solutions of SD36 and SD48 were spin-coated onto the template and annealed in a solvent annealing chamber at room temperature using toluene vapor for 8 and 12 h, respectively. After the self-assembly process, the samples were treated with CF_4 plasma to remove the top-segregated PDMS, followed by O_2 plasma to remove the PS matrix and to obtain the SiO_x line patterns.

S-nTP Process. PMMA homopolymer (MW = 100 kg mol⁻¹) was purchased from Sigma-Aldrich Inc., and it was dissolved in a mixed solvent of toluene, acetone, and heptane (4.5:4.5:1 by volume, 4 wt %). Before replication, the surface of the master molds was treated with a PDMS brush. A PMMA solution was spin-coated onto the master molds at 2500 rpm. A PI adhesive film (3 M Inc.) was then attached on the surface of the PMMA replica and detached from the mold with the inverted surface topography of the templates. Cr nanowires were fabricated by angled deposition of the Cr source onto the PMMA replica using an e-beam evaporator (deposition angle = 75°). The Cr nanowires/PMMA/PI adhesive film was exposed to a mixed solvent vapor of acetone and heptane (1:1 by volume) at 55 °C for 30 s and then brought into contact with receiver substrates. After the transfer printing process, the PMMA replica was washed with a mixed solvent of acetone and toluene (1:1 by volume). Similarly, Cr mesh nanostructures were obtained by sequential printing.

BCP Self-Assembly To Form SiO_x Nanodots. PS-*b*-PDMS (MW = 56 kg mol⁻¹, SD56) and a hydroxyl-terminated PDMS brush (MW = 5 kg mol⁻¹) were purchased from Polymer Source Inc. (Canada). Solutions of SD56 (1 wt %) and hydroxyl-terminated PDMS homopolymer (1.5 wt %) were prepared. For the directed self-assembly process, the sample was treated with a PDMS brush at 200 °C using a vacuum oven. The SD56 solution was spin-coated onto the sample; it was then thermally annealed in a vacuum oven at 150 °C for 2 h. After

the self-assembly process, the sample was treated with CF_4 plasma to remove the top-segregated PDMS, followed by O_2 plasma to remove the PS matrix and oxidize the PDMS dots, resulting in the SiO_x nanodots pattern.

ECM-Based Memristor Device Fabrication. Si substrates with 150 nm thick dry-oxidized SiO_2 were prepared. A Pt BE (100 nm)/Cr adhesion layer (20 nm) was deposited using a radio frequency sputtering system and patterned by a conventional optical lithography process. A SiO_2 solid electrolyte layer was deposited with plasma-enhanced chemical vapor deposition equipment using SiH_4 , N_2O , and Ar gases (for the conventional cell, 60 nm; for the SiO_x nanodot-incorporated cell, 60 nm; for the nanopatterned cell, 120 nm). For the nanopatterned cell, two kinds of Cr nanomesh masks (13 and 20 nm wide lines) were formed on the SiO_2 films with the S-nTP process. Only the 60 nm thick SiO_2 layer was asymmetrically etched through the Cr mesh mask using a reactive ion etching system with C_4F_8 gas. For the formation of SiO_x nanodots with a diameter of 20 nm, the aforementioned BCP self-assembly process was used. Finally, the Ag TE (20 nm) was deposited with a dc sputtering system and patterned with the photolithography process.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b04578.

Supplementary Figures S1–S12 (PDF)

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Notes

The authors declare no competing financial interest.

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