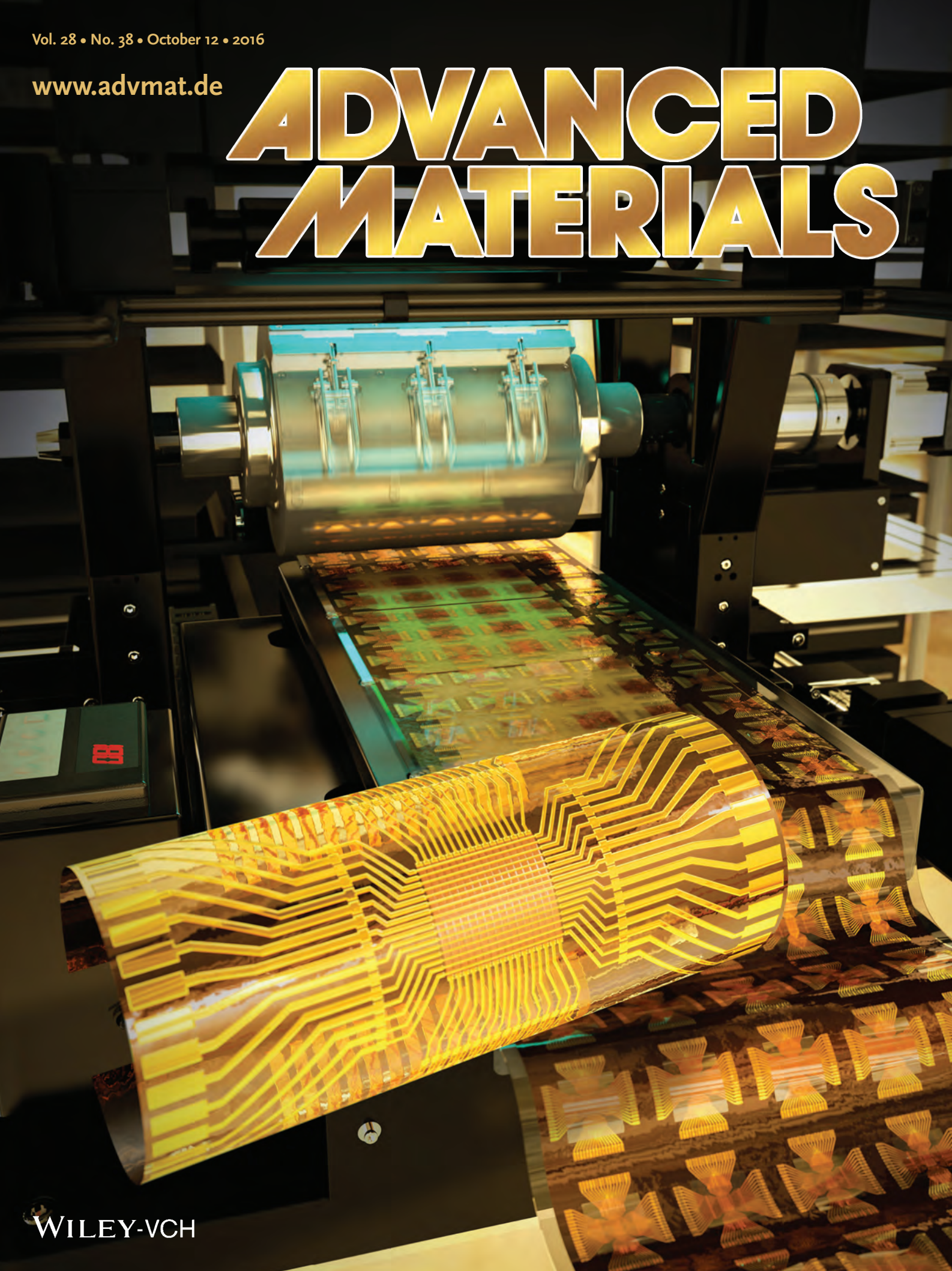
Vol. 28 • No. 38 • October 12 • 2016

www.advmat.de

ADVANCED MATERIALS



WILEY-VCH

Simultaneous Roll Transfer and Interconnection of Flexible Silicon NAND Flash Memory

Do Hyun Kim, Hyeon Gyun Yoo, Sung Min Hong, Bongkyun Jang, Dae Yong Park, Daniel J. Joe, Jae-Hyun Kim, and Keon Jae Lee**

Roll-based manufacturing is considered a key technology for mass production of unconventional flexible electronics[1] (e.g., rollable computers and wearable smart devices), enabling high-throughput, continuous, and cost-efficient processes.[2–4] Recently, a number of researchers have reported innovative advances in roll-to-roll (R2R) processing including graphene production,[5] surface nanotexturing,[6] nanoimprint lithography,[7,8] and transfer of oxide thin-film transistors (TFTs).[9] In order to realize roll-based flexible electronic systems, high-performance large-scale integrated circuits (LSI) (consisting of more than thousands of integrated nanotransistors) such as a flexible micro processing unit (f-MPU), high-density memory, and a wireless radio-frequency (RF) module should be continuously integrated on a flexible substrate utilizing a roll process for useful and complex computations.[10]

Flexible LSI (f-LSI) has attracted significant interest in developing advanced soft microprocessors,[11–13] data storage,[14] and communication devices[15] since most of the complicated functions are mainly performed by large numbers of high-speed integrated nanoscale transistors.[16] In this regard, single crystalline Si-based f-LSI has been extensively studied due to its outstanding properties (e.g., high carrier mobility, drive current, and thermal stability) and compatibility with the state-of-the-art CMOS technology.[17] In the recent past, several groups of researchers have exploited various methods such as controlled spalling[14,18] and a top-layer release technique[19,20] for Si-based flexible LSI devices. In 2013, our group reported the first demonstration of ultrathin Si-based f-LSI (active Si thickness of 145 nm) using a 0.18 μm CMOS process for wireless communication.[21] The f-LSI was successfully implemented because the LSI was initially fabricated on a bulk wafer and only the ultrathin LSI layer was transferred onto a flexible substrate, eliminating additional problematic multi-alignment and nanofabrication steps on plastics. Nonetheless, important challenges to realize essential operations (i.e., processing and storing data) and productive transfer of the f-LSI onto the plastic substrate remain.

In addition to the realization of f-LSI, its flexible packaging is another critical issue to be addressed to realize fully operational flexible systems by the interconnection of core and peripheral devices (e.g., MPU, memory, display, and battery).[22] Packaging is an advanced back-end process that entails assembling the LSI to be electrically functionalized for signal transmission and to be mechanically protected from external shocks.[23,24] In particular, flip-chip packaging by an anisotropic conductive film (ACF), which directly interconnects vertically aligned electrodes with conductive particles randomly dispersed in a resin-based matrix,[25] provides excellent elastic and resilient properties under bending conditions. In an earlier work, we utilized an ACF as a flexible packaging material for flexible AlGaInP light-emitting diodes (f-LEDs).[26] Nevertheless, little effort has been devoted to further develop the f-LSI packaging technology, in spite of increased importance of reliable integration in the upcoming era of flexible systems.

Herein, we demonstrate simultaneous roll transfer and interconnection of Si-based flexible NAND flash memory (f-NAND) based on highly productive roll-to-plate ACF packaging. An ultrathin f-NAND chip was prepared on an intermediate transfer substrate by bonding the Si NAND flash on a rigid glass and subsequently removing the handle wafer. Roll-based flip-chip packaging technology with precise optical alignment allowed the f-NAND to be transferred and simultaneously interconnected on a flexible printed circuit board (FPCB) through thermo-compression ACF bonding. The ACF packaging materials exhibited outstanding bonding capability for continuous roll-based transfer and excellent flexibility of interconnection, because of its inherent elastic nature from the polymer-based thermo-setting resin. Nonlinear elastic deformation of the dynamic roll-based bonding was investigated by a finite element analysis (FEA) to optimize the uniform pressure distribution on the FPCB with concentrated pressure on electrode bumps for reliable transfer and interconnection. Finally, the ACF-packaged Si f-NAND was successfully completed on the FPCB in a chip-on-flex structure, showing excellent flexibility and stable operations of the NAND memory. Unit flash memories with outstanding properties were connected in series to build a NAND flash string. Reliable operation of the flexible 16 × 16 NAND flash array was confirmed at the circuit level by programming and reading letters in ASCII codes. The results may open up new opportunities of integrating Si-based high-performance f-LSIs on plastics with the ACF packaging in highly productive roll-based production.

D. H. Kim, Dr. H. G. Yoo, D. Y. Park, Dr. D. J. Joe, Prof. K. J. Lee
Department of Materials Science and Engineering
Korea Advanced Institute of Science and Technology (KAIST)
291 Daehak-ro, Yuseong-gu
Daejeon 305-701, Republic of Korea
E-mail: keonlee@kaist.ac.kr

S. M. Hong, B. Jang, Dr. J.-H. Kim
Department of Nano Mechanics
Nano-Convergence Mechanical Systems Research Division
Korea Institute of Machinery and Materials (KIMM)
156 Gajeongbuk-ro, Yuseong-gu, Daejeon 305-343, Republic of Korea
E-mail: jaehkim@kimm.re.kr

DOI: 10.1002/adma.201602339

© 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

ADVANCED MATERIALS
www.advmat.de

www.MaterialsViews.com

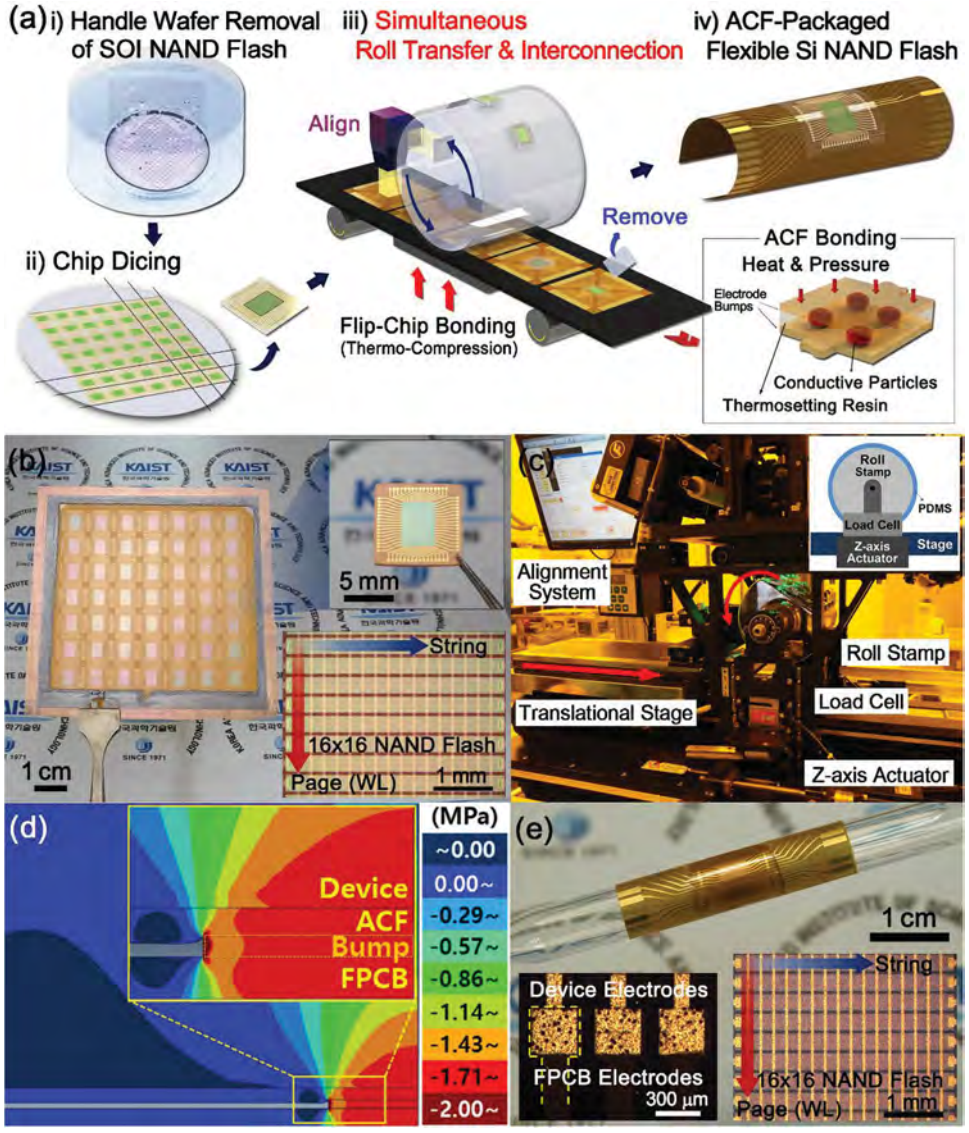


Figure 1. a) Fabrication procedure of the ACF-packaged flexible Si NAND flash memory by roll-based thermo-compression bonding. i) NAND flash fabrication on an SOI wafer and subsequent bonding with intermediate transfer glass. Handle wafer and BOX removal by mechanical and chemical thinning process. ii) NAND chip separation by dicing. iii) Roll-based transfer and simultaneous interconnection of the memory on an FPCB. iv) Completed ACF-packaged Si f-NAND. The inset illustrates the electrode bumps of the device and the FPCB, which are adhered and interconnected by thermosetting resin and conductive particles, respectively. b) Image of the ultrathin Si NAND devices on intermediate transfer glass with a magnified OM image (lower inset). The upper inset shows the diced device prepared for roll-based packaging. c) The R2P equipment for device transfer and simultaneous interconnection. The inset illustrates the side view. d) Contour plot of cross-sectional pressure distribution on electrode bumps simulated by nonlinear elastic deformation FEA in Case A. e) Photograph of the highly compliant ACF-packaged f-NAND wrapped on a glass rod (diameter of 7 mm). The OM image of the electrode area (left) and the active device area (right) are shown in insets.

Figure 1a illustrates the fabrication procedure of the ACF-packaged Si f-NAND. The charge-trap (CT) NAND flash memories based on an $Al_2O_3/Si_3N_4/Al_2O_3$ multi-layer stack are fabricated on a silicon-on-insulator (SOI) wafer (340 nm thick top-Si layer) by conventional CMOS process (as shown in Figure S1, Supporting Information). The top side of the SOI wafer is adhered to an intermediate transfer medium of a rigid glass substrate for further thinning process. Chemical-mechanical polishing (CMP) is applied to thin the wafer from 760 μm down to 200 μm. After the sealing, the remaining handle wafer (bottom-Si) and the buried oxide (BOX) layer are entirely eliminated by a potassium hydroxide (KOH) solution (65 °C, 30 wt%) and buffered oxide etchant (BOE) (10:1 diluted HF), respectively. Large selectivity of etchants limits the excessive etching of each material,[27] resulting in a highly uniform ultrathin device layer without any damage. The device contact electrode is exposed from the bottom side after BOX removal. After dicing, the f-NAND is transferred and simultaneously interconnected on an FPCB (30 μm thick polyimide substrate with Cu electrode) by roll-to-plate

© 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

flip-chip packaging of ACF thermo-compression bonding. By removing the intermediate transfer glass through light-induced lift-off technique,[28,29] ACF-packaged flexible Si NAND flash is completed.

Figure 1b is a photograph of the ultrathin Si NAND flash memories prepared on an intermediate transfer glass of a hard supporter during the harsh roll-based interconnection process. Epoxy-based adhesive between a device wafer and a transfer glass effectively prevents wafer warpage and structural damage during the etching and the transfer process,[30] as shown in the optical microscopy (OM) image (lower inset). The upper inset shows the diced transfer glass separating the individual flash chip for roll-based transfer and packaging. Note that our process undergoes batch wafer thinning followed by dicing, which eliminates the time-consuming process of multiple etching steps and facilitates a high-throughput roll process.

In order to achieve reliable packaging, thermo-compression bonding of ACF materials softens and spreads the polymer matrix to adhere the LSI chip onto the FPCB, and concurrently compresses the conductive particles between electrode bumps to construct electrical paths,[25] as shown in the inset of Figure 1a. The roll packaging process of f-LSI needs to be well-optimized to avoid an irregular stress distribution originating from the roll nip pressure, causing improper interconnections and damage of the fragile ultrathin Si chip.[9] Figure 1c and the inset show a roll-to-plate equipment for the simultaneous transfer and interconnection of the f-LSI, consisting of a motor-driven roll-stamp, two *Z*-axis actuators with load sensors for pressure control, and a heating translational flat-stage with three degrees of motional freedom (*X*-axis and *Y*-axis displacements, and *Z*-axis angular rotation) for precise alignment. 4 mm thick poly(dimethylsiloxane) (PDMS) sheet is wrapped around the roll to achieve conformal contact with tailored nip pressure and adhesion for the pick-and-place process. The roll-based interconnection proceeds as follows: i) laminating the ACF on an FPCB, ii) placing the f-NAND and the FPCB on a roll-stamp and a translational stage, respectively, iii) optically aligning the electrodes, and iv) conducting flip-chip thermo-compression ACF bonding for transferring f-NAND on the FPCB (see Video S1, Supporting Information). Note that our process eliminates further troublesome interconnection process on ultrathin Si-based device by introducing ACF packaging material in the transfer step. The roll-stamp contact pressure on the translational stage is controlled by *Z*-axis actuators with a real-time load feedback system to maintain the prescribed load value to ensure the optimum bonding conditions. It is important to synchronize the roll-stamp rotation speed and the translational stage velocity for minimizing relative motions and preventing misalignment, device damage, and shear deformation of the ACF. In addition, the bonding speed has to be optimized with process temperature to achieve the ACF interconnection. The roll transfer is performed at the speed of 1 mm s^{-1} under 170 °C, which can be increased without losing accuracy up to 5 mm s^{-1} at higher temperature. This continuous roll-to-plate ACF packaging provides excellent process continuity with highly productive roll-based manufacturing compared to the conventional static die bonding technique.

Highly concentrated pressure on electrode bumps is required for electrical interconnections of ACF since the conductive particles should be sufficiently compressed to increase the contact area between the bumps and the particles. From the mechanics point of view, elastic matching of the bonding stack, related to the order of the pressurized components (i.e., PDMS, FPCB, ACF, and f-NAND (on transfer glass)), is a particularly important technology to attain pressure concentration on the bumps during highly productive roll process. Nonlinear elastic deformation with respect to the applied pressure is simulated using a finite element code (ABAQUS, Dassault Systemes) depending on two different types of bonding stacks; the f-NAND and the FPCB are placed on a roll-stamp and a translational stage, respectively (Case A), or the opposite (Case B), as shown in Figure S2 (Supporting Information) (material properties used in the simulation are listed in Table S1, Supporting Information). The same amount of external load is applied to both cases in FEA. As shown in the cross-sectional pressure distribution of Figure 1d and Figure S3 (Supporting Information), the electrode bump in Case A experiences concentrated pressure over 1.8 MPa for the critical value of ACF interconnection, whereas the bonding stack of Case B results in the homogenized bump pressure except for a stress gradient at the bump edge. The process window is investigated up to 6 MPa without any device fracture nor improper interconnection, which is relatively wide due to the well-organized elastic matching of the bonding stack. Therefore, the stack order of Case A is an optimum configuration for our roll-to-plate flip-chip bonding.

The ACF-packaged f-NAND after being released from the transfer glass is shown in Figure 1e. Ultrathin Si-based flexible memory with the elastic ACF interconnection achieves large flexibility and conformal attachment on a curved surface of a 7 mm diameter glass rod. The left inset shows an OM image of the electrodes properly aligned and interconnected with each other (black dots on the electrodes are from compressed ACF conductive particles). The right inset is an OM image of the active area of the 16 × 16 flexible NAND array. No mechanical damage such as cracks or wrinkles appeared on the entire f-NAND area. In addition, there is no observed destructive effect from the conductive particles since only the particles within the electrode area are compressed due to the electrode bump height, while the others are remained uncompressed, as shown in Figure S4 (Supporting Information).

Accurate alignment is necessary for roll-based transfer and interconnection since imprecise positioning reduces the overlapped electrode area and increases the contact resistance. **Figure 2**a schematically illustrates the alignment method of our roll-to-plate equipment. Two microscopes initially detect the alignment marker position on the FPCB (denoted as A and B) and a device (denoted as a and b), respectively. Based on the computational results with internal feedback, the translational stage automatically moves in the *X*- and *Y*-directions with angular *Z*-axis rotation to align the f-NAND and the FPCB within 5 μm accuracy.

Figure 2b is a bonding stack illustration of Case A, where the f-NAND (on a transfer glass) and the FPCB are placed on a roll-stamp and a plate (translational stage), respectively. The

© 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

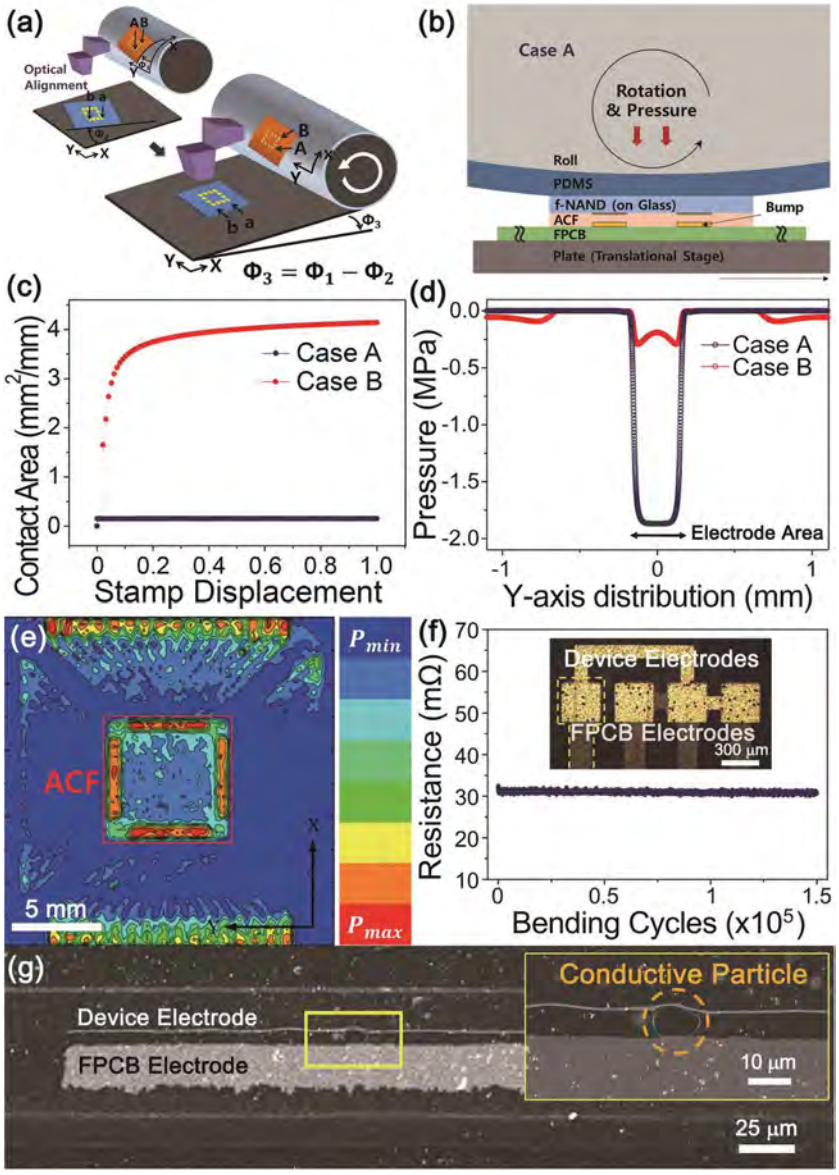


Figure 2. a) A schematic illustration of the alignment method to precisely position the device electrodes with the corresponding FPCB electrodes. b) Bonding stack of Case A determined for our roll-to-plate packaging process. c) Simulated contact area with respect to the normalized stamp displacement. d) Simulated pressure on the electrode bump as a function of *Y*-axis distribution. e) Pressure distribution measurement results on the FPCB in Case A. f) Contact resistance as a function of the bending cycles. The data points were obtained every ten cycles of bending. The inset shows the OM image of the electrode area of the test sample. g) The cross-sectional SEM image of the electrode area showing a finely captured conductive particle between the electrodes, which is the effective current path.

broadening of the pressurized region resulting from structural deformation is undesirable during roll bonding since it causes a significant decrease in the bump pressure leading to interconnection failure. The rigid transfer glass and the plate of Case A effectively prevent the structural deformation of f-NAND and the FPCB, which restricts the pressurized area and concentrates the pressure on electrode bumps for ACF interconnection. Figure 2c,d shows the simulated contact area and pressure on the FPCB during dynamic roll-based compression for two different bonding stack orders, Case A and Case B. Due to the limited size of contact area, highly concentrated bump pressure of Case A (1.87 MPa) exceeded the minimum pressure required for ACF bonding (1.8 MPa) with improved uniformity for outstanding interconnection. Figure 2e (Case A) and Figure S5 (Supporting Information) (Case B) show the experimental measurement of the pressure distribution, visualized by a pressure-sensitive paper (Prescale, Fujifilm). The experimental results are consistent with the previous simulated data in Figure 2d, ensuring a uniform chip and concentrated bump pressure for reliable roll transfer and interconnection. Low contact resistance and stable operation of the ACF interconnection are crucial for repeated bending cycles of the f-LSI. Figure 2f shows the contact resistance measured by the four-point probe method as a function of 1.5×10^5 bending cycles at a 5 mm bending radius without significant changes in the resistance, due to the resilient nature of the ACF packaging material. The inset of Figure 2f shows an OM image of the electrode area where the upper device electrodes and the lower FPCB electrodes are connected for the four-point probe test. A cross-sectional scanning electron microscope (SEM) image of the electrode area is shown in Figure 2g. The compressed conductive particles between the device and FPCB electrodes are observed as an effective current path. The final device forms a chip-on-flex (COF) structure, providing outstanding flexibility with mechanical stability even with harsh bending.[22]

Figure 3a shows a schematic illustration and a cross-sectional transmission electron microscopy (TEM) image of the flash memory unit cell. The memory consists of a silicon source(n^+)/channel(p)/drain(n^+) region (channel length of 15 μm and width of 250 μm) and an $Al_2O_3/Si_3N_4/Al_2O_3$ charge-trap multilayer stack (3 nm thick Al_2O_3 tunneling oxide, 8 nm thick Si_3N_4 CT layer, and 15 nm thick Al_2O_3 blocking oxide). Reliable operation of a flexible unit flash memory is important for NAND array integration since the NAND string is a series connection of unit memory cells along a bit line, and insufficient unit cell performance can interrupt the series current or disable the entire string. Figure 3b shows hysteresis in the transfer curve of the flexible unit flash memory.[31] A voltage pulse of –16 V/0.5 s was applied to the control gate for the initial erase operation. Gradual increments in maximum gate voltages (V_g) applied for program operation (from 4 to 14 V) resulted in a wider memory window due to the increased

© 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

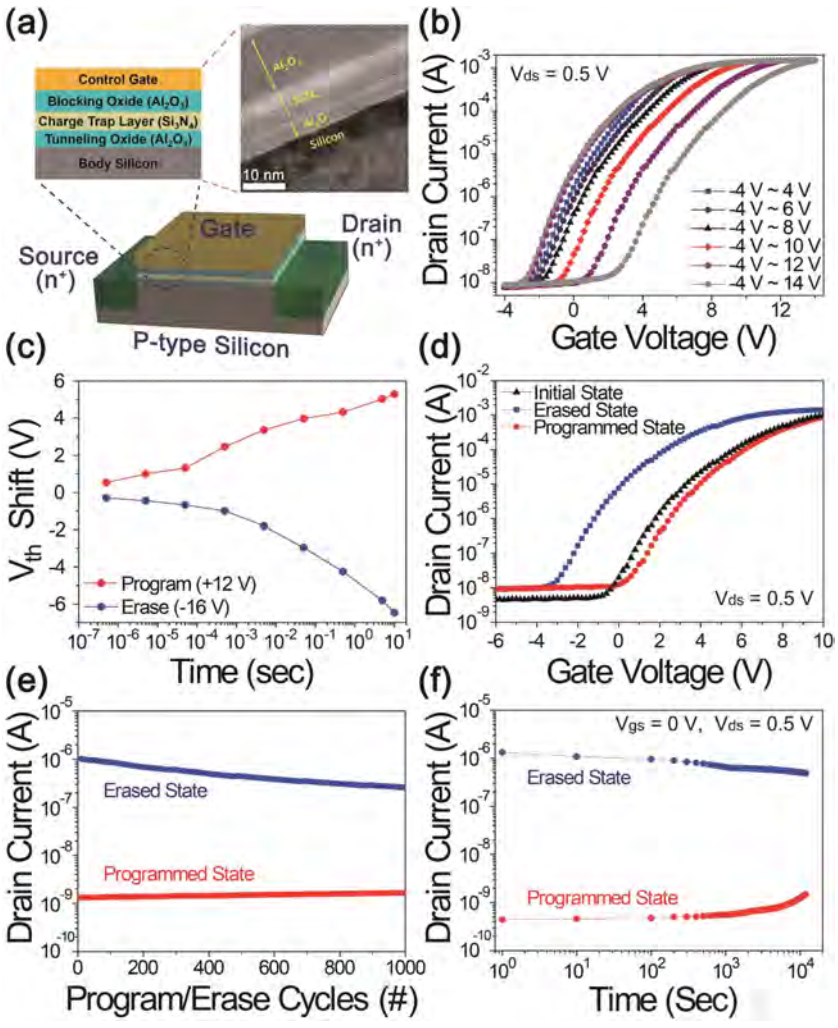


Figure 3. a) Schematic illustration of the flash memory unit cell and TEM image of Al_2O_3/Si_3N_4/Al_2O_3 multilayer thin films deposited on silicon. b) Obtained double transfer curve of the CT flash memory with increasing V_g for program operation. c) The V_{th} shift plots of the fabricated memory as a function of the voltage pulse width. d) The determined hysteresis transfer curve of the flash memory for the NAND operation. e) Endurance and f) retention test results of the fabricated CT flash memory.

electrons in the trap site. In Figure 3c, the threshold voltage (V_{th}) shift was investigated as a function of applied V_g pulse width. The memory cell was initially erased or programmed prior to the program or erase operation, respectively. Increasing the V_g pulse width (from 5×10^{-7} s to 10 s) gradually shifted the V_{th} to negative (at −16 V for erase) or to positive (at +12 V for programming) direction, exhibiting the CT characteristics of the flash memory.

To operate the NAND flash memory, erased and programmed unit cells were set to have a negative and positive V_{th}, respectively.[32] In order to satisfy these criteria, the voltage pulse of −16 V/0.5 s for erase operation followed by +12 V/0.5 s for program operation were applied to the initial state cell. Figure 3d shows the transfer curve hysteresis of the unit memory cell at a drain voltage of 0.5 V, indicating a high I_{on}/I_{off} ratio greater than 10^3 at zero read gate voltage. Figure 3e,f shows the endurance and retention properties of the flexible unit flash memory, respectively, presenting stable and reversible memory characteristics with a high I_{on}/I_{off} ratio of over 100 during 1000 cycles of program/erase switching and 10^4 s duration.

Figure 4a is the cross-sectional circuit diagram of the NAND flash string composed of 16 flash memory cells connected in series. Each memory cell in a NAND string can be classified as a selected (SC) or an unselected cell (USC) in program and read operation. Figure 4b describes a NAND flash string for each of four measurement conditions. To address an SC, all of other USC in the string need to be ON as a pass transistor, regardless of their programmed or erased state. In order to determine the pass voltage (V_{pass}), the string current (I_{string}) of the four different cases was measured as a function of the applied V_g. As shown in Figure 4c, there is a large difference in I_{string} depending on whether the selected cells are erased ((1), (2)) or programmed ((3), (4)) state at 6 V or higher. Figure 4d shows the I_{string} of the flexible NAND flash string according to the erased and programmed state. The bit line voltage was swept from 0 to 5 V to evaluate the I_{string}, while 0 and 6 V were applied for the selected and the other word lines, respectively. The large difference in the I_{string} between the programmed and erased states was observed due to the high I_{on}/I_{off} ratio of the f-NAND unit cell. The circuitry operation of f-NAND was successfully achieved throughout the entire array (16 × 16) without any degraded cells, due to the outstanding performance of Si-based memories with stable ACF interconnection.

The 16 × 16 f-NAND was realized by integrating 16 NAND strings through word lines. To confirm the data storage capability of the f-NAND, the ASCII character code was used in programming operation to record alphabet letters. For example, the letter "K" was programmed as a corresponding ASCII code "01001011." **Figure 5**a demonstrates that the device successfully retained the ten-character long ASCII code of "KAIST&KIMM," showing a distinct I_{string} difference with a ratio of higher than 30. Note that the I_{on}/I_{off} ratio of the unit flash memory (>100) was reduced to ≈30 due to the series resistance of the f-NAND string. The utilization of the latest NAND flash integration technology including advanced fabrication processes, materials,[33,34] and memory structures,[35,36] and their optimization in terms of device flexibility can improve the performance of the f-NAND.

To evaluate its mechanical reliability, the current of an entirely erased and programmed string was measured during bending tests. Figure 5b shows that the NAND flash memory maintained its I_{string} ratio during 1000 repetitive bending (5 mm

© 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

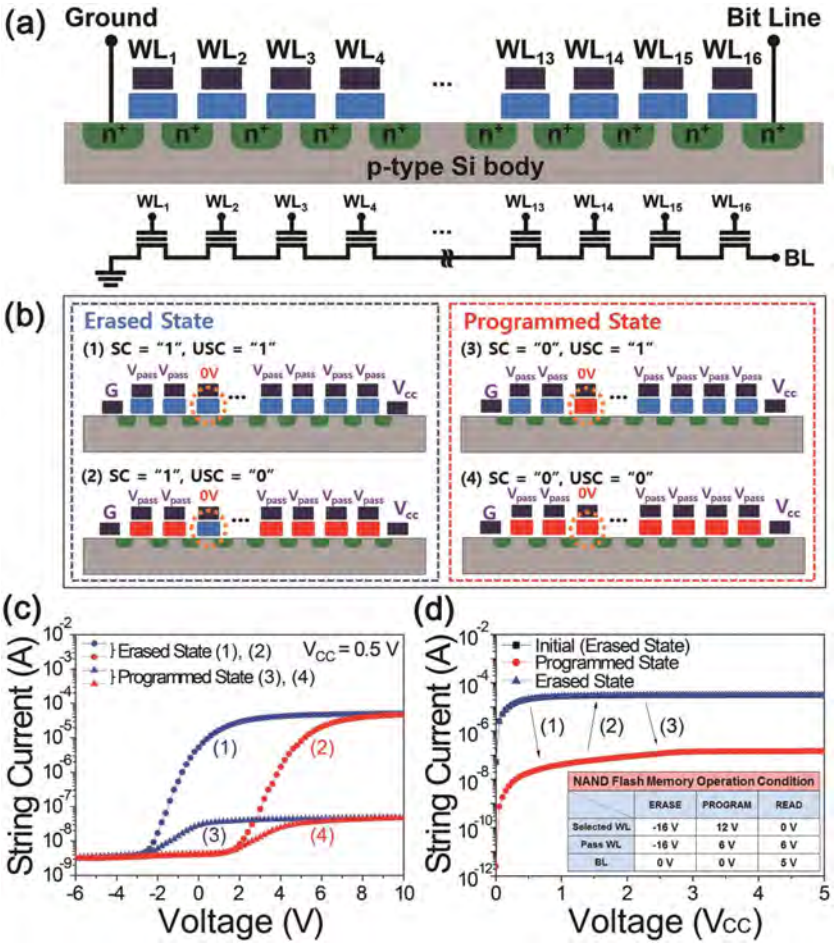


Figure 4. a) Cross-sectional schematic and the circuit diagram of the flexible silicon NAND flash string composed of 16 unit flash memory cells in series. b) A simple illustration of NAND flash string for each of four measurement conditions ((1), (2), (3), (4)). c) The string current of flexible NAND flash string as a function of applied pass voltage. There is a distinct difference in the string current depending on whether the selected cells are erased (1,2) or programmed (3,4) states at 6 V or higher. On the contrary, the states of unselected cells do not affect the string current value. d) The NAND flash string current according to the erased and programmed states. The inset table shows operation conditions for the NAND flash string.

of bending radius) cycles without any performance degradation. Similarly, the I_{string} ratio between the erased and programmed states was maintained irrespective of the bending radii from 50 to 5 mm, as shown in Figure 5c. These experimental results confirm sufficient mechanical stability of the ACF packaged f-NAND. To the best of our knowledge, this is the first circuitry level demonstration of ultrathin Si-based f-NAND with the ACF interconnection.

In conclusion, we have successfully demonstrated Si-based flexible NAND flash memory applying roll-to-plate flip-chip packaging technology. The roll-based thermo-compression bonding of ACF together with elastic matching technique enables an ultrathin f-NAND to be transferred and simultaneously interconnected on an FPCB using a roll process. An FEA simulation of nonlinear elastic deformation validated that the elastically matched stack order of the roll-to-plate ACF interconnection was the f-NAND and FPCB placed on the roll-stamp and translational stage (Case A), respectively. Contact pressure measurements of Case A also confirmed that the pressure was symmetrically distributed with excellent control on the FPCB and optimally concentrated on the electrode bumps over 1.8 MPa for the ACF interconnection. The reliability of the flexible ACF packaging was confirmed through a four-point probe test during 1.5×10^5 repetitive bending cycles. Unit flash memories with outstanding properties (e.g., high I_{on}/I_{off} ratio (>10^2 at V_{read}), reproducible endurance (>10^3 switching cycles), and long retention (>10^4 s)) were connected in series to form a NAND flash string. The final 16×16 f-NAND exhibited stable operation and reliable addressing up to a bending radius of 5 mm. Our technology provides an innovative method to integrate state-of-the-art CMOS f-LSI devices on plastics using a highly productive roll process. These results can also be extended to the development of all-in-one integration of f-MPUs, high-density memories (e.g., 3D NAND flash memory), displays, and energy sources on plastics through ACF interconnection, which will be a crucial technology to achieve fully flexible electronics.

Experimental Section

Silicon NAND Flash Memory Fabrication: NAND flash memory was fabricated on a p-type (boron doped; 10–20 Ω cm) SOI wafer (Unibond, SOITEK) consisting of a 340 nm (100) orientation top silicon layer, a 1 μm BOX layer, and a thick bottom silicon layer (handle wafer). The wafer was initially prepared by sequential ultrasonic cleaning by acetone, isopropyl alcohol (IPA), and deionized (DI) water. A heavily n-doped region was formed on the p-type top Si layer utilizing spin-on-dopant (P509, Filmtronic) for the transistor source/drain region (channel length of 15 μm and channel width of 250 μm). A photo-lithographically defined SiO_2 layer, deposited by plasma-enhanced chemical vapor deposition (PECVD), was used as a doping mask. Thereafter, isolation along the NAND flash string direction was made by SF_6 plasma reactive ion etching (RIE) to prevent the leakage current. A 3 nm Al_2O_3 tunneling oxide, an 8 nm Si_3N_4 charge trap layer, and a 15 nm Al_2O_3 blocking oxide layer were subsequently deposited for charge-trap flash memory characteristics. The tunneling and blocking Al_2O_3 oxide layer and the charge trapping Si_3N_4 layer were deposited by plasma-enhanced atomic layer deposition (PEALD) and PECVD, respectively. After forming contact holes by BOE, the layer of Au/Cr (200 nm/10 nm) for gate, source, and drain electrodes was deposited using RF sputtering. The state-of-the-art materials such as TANOS(SiO_2–SiN–Al_2O_3–TaN) or SONOS(poly Si–SiO_2–Si_3N_4–SiO_2–Si) can further improve the memory performance.[33,34]

Intermediate Transfer Glass Removal: A light-induced lift-off technique was used to detach the ultrathin Si f-NAND from the transfer glass. As an intermediate transfer medium, a glass substrate (Corning Glass, 700 μm in thickness) was utilized.

Device Measurements: All electrical characterizations were conducted using a Keithley 4200-SCS semiconductor measurement system with a

© 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

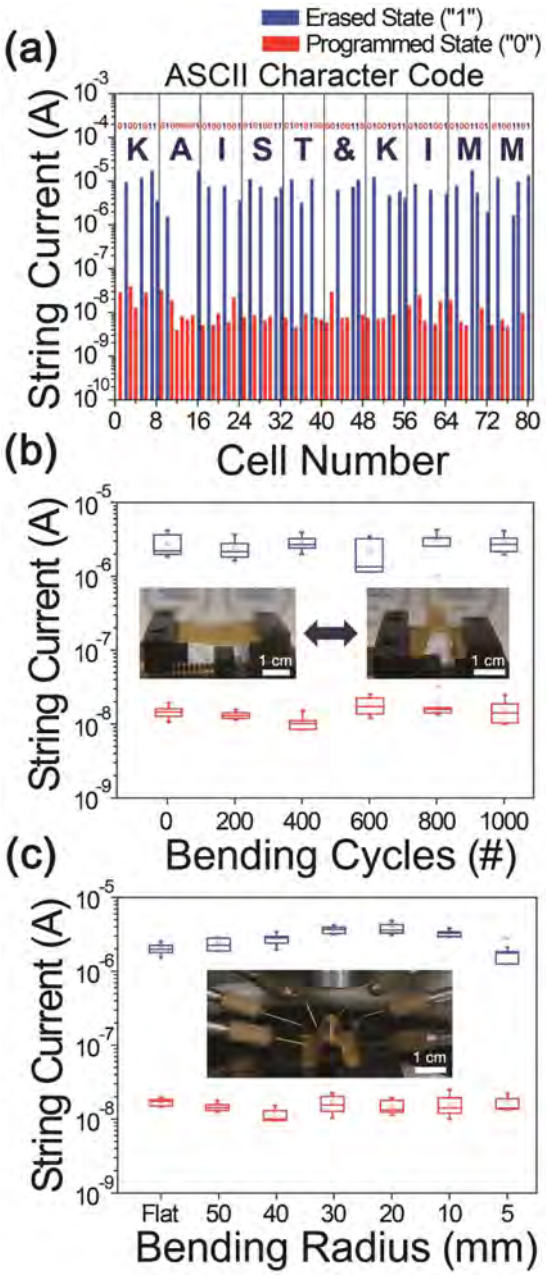


Figure 5. a) The NAND flash string current histogram showing the words "KAIST&KIMM" with standard ASCII character codes within the 80 bit flexible NAND flash memory. b) Bending fatigue test results of the flexible NAND flash memory during 1000 bending cycles. c) The string current of the programmed and erased states as a function of bending radius. (Erased state "1" and programmed state "0" are denoted by blue and red, respectively, for all of (a), (b), and (c).)

pulse measurement unit (Keithley 4225-PMU) and a remote amplifier/switch (Keithley-4225-RPM).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

D.H.K. and H.G.Y. contributed equally to this work. This work was supported by the internal research program "Development of Infrastructure for Flexible Devices with High-Performance Using Nanomaterials (SC1170)" of Korea Institute of Machinery and Materials, and the National Research Foundation of Korea (NRF) grant funded by the Korean Government (MSIP) (NRF-2016R1A5A1009926).

Received: May 2, 2016
Revised: June 27, 2016
Published online: July 20, 2016

[1] W. S. Wong, A. Salleo, *Flexible Electronics: Materials and Applications*, Springer Science+Business Media LLC, New York **2009**.
[2] H.-J. Kim, M. Almanza-Workman, B. Garcia, O. Kwon, F. Jeffrey, S. Braymen, J. Hauschildt, K. Junge, D. Larson, D. Stieler, A. Chaiken, B. Cobene, R. Elder, W. Jackson, M. Jam, A. Jeans, H. Luo, P. Mei, C. Perlov, C. Taussig, *J. Soc. Inf. Disp.* **2009**, *17*, 963.
[3] K. Jain, M. Klosner, M. Zemel, S. Raghunandan, *Proc. IEEE* **2005**, *93*, 1500.
[4] J. D. Morse, presented at NIST-NNN Workshop, Boston, MA, September **2011**.
[5] S. Bae, H. Kim, Y. Lee, X. F. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Ozyilmaz, J.-H. Ahn, B. H. Hong, S. Iijima, *Nat. Nanotechnol.* **2010**, *5*, 574.
[6] M. H. Lee, N. Lim, D. J. Ruebusch, A. Jamshidi, R. Kapadia, R. Lee, T. J. Seok, K. Takei, K. Y. Cho, Z. Y. Fan, H. Jang, M. Wu, G. Cho, A. Javey, *Nano Lett.* **2011**, *11*, 3425.
[7] S. H. Ahn, L. J. Guo, *Adv. Mater.* **2008**, *20*, 2044.
[8] S. H. Ahn, L. J. Guo, *ACS Nano* **2009**, *3*, 2304.
[9] B. K. Sharma, B. Jang, J. E. Lee, S.-H. Bae, T. W. Kim, H.-J. Lee, J.-H. Kim, J.-H. Ahn, *Adv. Funct. Mater.* **2013**, *23*, 2024.
[10] A. Nathan, A. Ahnood, M. T. Cole, S. Lee, Y. Suzuki, P. Hiralal, F. Bonaccorso, T. Hasan, L. Garcia-Gancedo, A. Dyadyusha, S. Haque, P. Andrew, S. Hofmann, J. Moultrie, D. P. Chu, A. J. Flewitt, A. C. Ferrari, M. J. Kelly, J. Robertson, G. A. J. Amaratunga, W. I. Milne, *Proc. IEEE* **2012**, *100*, 1486.
[11] B. Crone, A. Dodabalapur, Y.-Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, W. Li, *Nature* **2000**, *403*, 521.
[12] D. M. Sun, M. Y. Timmermans, Y. Tian, A. G. Nasibulin, E. I. Kauppinen, S. Kishimoto, T. Mizutani, Y. Ohno, *Nat. Nanotechnol.* **2011**, *6*, 156.
[13] D. K. Kim, Y. M. Lai, B. T. Diroll, C. B. Murray, C. R. Kagan, *Nat. Commun.* **2012**, *3*, 1216.
[14] D. Shahrjerdi, S. W. Bedell, *Nano Lett.* **2013**, *13*, 315.
[15] C. Wang, J. C. Chien, K. Takei, T. Takahashi, J. Nah, A. M. Niknejad, A. Javey, *Nano Lett.* **2012**, *12*, 1527.
[16] J. P. Rojas, G. A. T. Sevilla, M. M. Hussain, *Sci. Rep.* **2013**, *3*, 2609.
[17] A. M. H. a. M. M. Hussain, *Adv. Mater.* **2016**, *28*, 4219.
[18] Y. J. Zhai, L. Mathew, R. Rao, D. W. Xu, S. K. Banerjee, *Nano Lett.* **2012**, *12*, 5609.
[19] J. P. Rojas, G. A. T. Sevilla, M. T. Ghoneim, S. Bin Inayat, S. M. Ahmed, A. M. Hussain, M. M. Hussain, *ACS Nano* **2014**, *8*, 1468.
[20] G. A. T. Sevilla, M. T. Ghoneim, H. Fahad, J. P. Rojas, A. M. Hussain, M. M. Hussain, *ACS Nano* **2014**, *8*, 9850.
[21] G. T. Hwang, D. Im, S. E. Lee, J. Lee, M. Koo, S. Y. Park, S. Kim, K. Yang, S. J. Kim, K. Lee, K. J. Lee, *ACS Nano* **2013**, *7*, 4545.
[22] K. L. Suk, H. Y. Son, C. K. Chung, J. D. Kim, J. W. Lee, K. W. Paik, *Microelectron. Reliab.* **2012**, *52*, 225.
[23] J. N. Burghartz, W. Appel, H. D. Rempp, M. Zimmermann, *IEEE Trans. Electron Devices* **2009**, *56*, 321.

© 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

[24] W. Christiaens, E. Bosman, J. Vanfleteren, *IEEE Trans. Compon. Packag. Technol.* **2010**, *33*, 754.
[25] D. Lu, C. P. Wong, *Materials for Advanced Packaging*, Springer Science+Business Media LLC, New York **2009**.
[26] C. K. Jeong, K. I. Park, J. H. Son, G. T. Hwang, S. H. Lee, D. Y. Park, H. E. Lee, H. K. Lee, M. Byun, K. J. Lee, *Energy Environ. Sci.* **2014**, *7*, 4035.
[27] K. R. Williams, R. S. Muller, *J. Microelectromech. Syst.* **1996**, *5*, 256.
[28] T. Ueda, M. Ishida, M. Yuri, *Jpn. J. Appl. Phys.* **2011**, *50*, 041001.
[29] W. S. Wong, T. Sands, N. W. Cheung, M. Kneissl, D. P. Bour, P. Mei, L. T. Romano, N. M. Johnson, *Appl. Phys. Lett.* **1999**, *75*, 1360.
[30] Y. Kim, S. K. Kang, S. E. Kim, *Microelectron. Reliab.* **2010**, *50*, 1988.
[31] P. Pavan, R. Bez, P. Olivo, E. Zanoni, *Proc. IEEE* **1997**, *85*, 1248.
[32] K. J. Baeg, D. Khim, J. Kim, B. D. Yang, M. Kang, S. W. Jung, I. K. You, D. Y. Kim, Y. Y. Noh, *Adv. Funct. Mater.* **2012**, *22*, 2915.
[33] M. H. White, D. A. Adams, J. K. Bu, *IEEE Circuits Device* **2000**, *16*, 22.
[34] S. Jeon, J. H. Han, J. H. Lee, S. Choi, H. Hwang, C. Kim, *IEEE Trans. Electron Devices* **2005**, *52*, 2654.
[35] S. Aritome, *NAND Flash Memory Technologies*, Wiley, Hoboken, NJ, USA **2016**.
[36] K. T. Park, S. Nam, D. Kim, P. Kwak, D. Lee, Y. H. Choi, M. H. Choi, D. H. Kwak, D. H. Kim, M. S. Kim, H. W. Park, S. W. Shim, K. M. Kang, S. W. Park, K. Lee, H. J. Yoon, K. Ko, D. K. Shim, Y. L. Ahn, J. Ryu, D. Kim, K. Yun, J. Kwon, S. Shin, D. S. Byeon, K. Choi, J. M. Han, K. H. Kyung, J. H. Choi, K. Kim, *IEEE J. Solid-State Circuit* **2015**, *50*, 204.

© 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim