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Performance Enhancement of Electronic and Energy Devices via Block Copolymer Self-Assembly

*Hyeon Gyun Yoo, Myunghwan Byun, Chang Kyu Jeong, and Keon Jae Lee**

The use of self-assembled block copolymers (BCPs) for the fabrication of electronic and energy devices has received a tremendous amount of attention as a non-traditional approach to patterning integrated circuit elements at nanometer dimensions and densities inaccessible to traditional lithography techniques. The exquisite control over the dimensional features of the self-assembled nanostructures (i.e., shape, size, and periodicity) is one of the most attractive properties of BCP self-assembly. Harmonic spatial arrangement of the self-assembled nanoelements at desired positions on the chip may offer a new strategy for the fabrication of electronic and energy devices. Several recent reports show the great promise in using BCP self-assembly for practical applications of electronic and energy devices, leading to substantial enhancements of the device performance. Recent progress is summarized here, with regard to the performance enhancements of non-volatile memory, electrical sensor, and energy devices enabled by directed BCP self-assembly.

1. Introduction

Advances in nanotechnology are essential for achieving continuous performance improvement in various devices, such as memory,[1] energy sources,[2] light-emitting diodes,[3] and electric sensors.[4] These advances are also important when attempting to downscale the device size.[5,6] Particularly, spatially defined nanoscale patterns or sacrificial templates applicable to diverse types of electronic and energy devices have been intensively studied as alternatives to optimize device-performance levels and to present an innovative solution for unresolved key issues, such as power reduction of phase change memory devices,[7] reliability improvements in resistive random-access-memory devices,[8] sensitivity increments in sensor devices,[9] and efficiency enhancements of energy-harvesting devices.[10] Spatial placement of the nanoscale elements at desired positions on the chip is of great importance when attempting to realize performance enhancements in electronic and energy devices.[11–17]

In a clear comparison with conventional lithography based on photoresist materials, as widely used for semiconductor fabrication, various types of alternative patterning techniques have been introduced in an effort to improve the pattern resolution, which is limited with regard to light diffraction.[18–22] electron-beam (e-beam) lithography,[18] nanoimprinting,[19] and directed BCP self-assembly,[21,22] considered as "next-generation lithographic techniques", have emerged as promising candidates for achieving well-defined surface patterns on the nanometer scale. Although e-beam lithography can easily produce nanometer-scale patterns, its practical use is restricted due to its low throughput and high fabrication costs.[21] Nanoimprinting is suitable to some extent for mass production, but it requires a costly master template.[23] On the other hand, BCP self-assembly based on the spontaneous microscopic phase separation of covalently linked polymer blocks has garnered tremendous interest as a powerful tool for autonomously achieving regular nanopatterns at short- and long-range order.[21,22,24,25] It is widely acknowledged that the shape of the self-assembled BCP nanodomain (i.e., spheres, perforated lamellae, cylinders, gyroidal, and lamellar structures) can be tuned simply by changing their molecular weight and composition, as depicted in **Figure 1**a.[26] Strongly depending on the Flory–Huggins interaction parameter (χ), the volume fraction of the components (f), and the degree of polymerization (N), the equilibrium morphologies of self-assembled BCP nanodomains can be categorized into body-centered-cubic spheres, hexagonally packed cylinders, bicontinuous gyroids, and lamellae (Figure 1b).[26] Most studies of BCP self-assembly have investigated the creation of regular arrays of features on a scale of 5–20 nm so as to open up a promising path for high-resolution lithography.[27–32] The international technology roadmap for semiconductors (ITRS) highlights directed self-assembly (DSA) as a potential option for sub-16 nm half-pitch nodes.[33] In addition, Cheng et. al. reports that the implementation of DSA combined with conventional ArF lithography for sub-10 nm resolution in 300 mm wafers.[32] Recently, spatially ordered nanostructures with a line width of 8 nm and a period of 17 nm were developed by means of the directed self-assembly of a poly(styrene-*block*-dimethylsiloxane) (PS-*b*-PDMS) BCP with a high-χ parameter (Figure 1c),[27] and a highly tunable pattern geometry (i.e., a minimum line width of 6 nm) has also been reported by researchers who used a poly(2-vinylpyridine-*block*-dimethysiloxane) (P2VP-*b*-PDMS) BCP with an extremely high-χ parameter (Figure 1d).[28] Bottom-up directed BCP self-assembly can offer a large-area, size-tunable, and cost-effective means of forming nanoscale patterns or templates, and this

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process is compatible with the top-down conventional complementary metal-oxide-semiconductor (CMOS) process.[7] Although remarkable progress in self-assembled BCP nanostructures has been achieved thus far, practical demonstration of self-assembled BCP nanoscale patterns or templates for electronic and energy devices are still in their infancy. More recently, research in which self-assembled patterns or templates were applied to actual devices has been proposed to improve device performance levels and solve the serious problems with regard to device operation, which have been major challenges in the area of self-assembled nanotechnology.[7–10]

This review discusses recent progress made in the use of self-assembled BCP nanostructures for electronic and energy applications, including next-generation non-volatile memory,[7,8,34–36] electrical sensors,[9,23] triboelectric nanogenerators,[10] and dye-sensitized solar cells,[37,38] considering how the device performance can be more effectively enhanced by adopting BCP self-assembly nanotechnology. A new fabrication strategy combined with the BCP self-assembly process will provide a novel outlook on the further development of electronic and energy devices.

2. Next-Generation Non-volatile Memory Devices

2.1. Phase-Change Memory (PCM) Devices

Phase-change memory (PCM) is one of the alternative types of memory that can replace flash memory in next-generation non-volatile memory devices.[39–41] A phase-change material such as chalcogenide $Ge_2Sb_2Te_5$ (GST) can be reversibly shifted between its crystalline and amorphous states through heating by applying appropriate voltage pulses, which causes a change in the resistance state.[40,42] The figure of merit, with high switching speed, good endurance, excellent retention properties, low fabrication cost, and inherent scalability, makes PCM more appealing than flash memory.[42]

In order to apply PCM practically as the core memory in consumer electronic devices, the main obstacle to overcome is the need to decrease the high writing reset current.[39,43] Making the contact area between the phase-change material and the heater electrode smaller would be one of the best ways to reduce the writing current in PCM.[11,44,45] Given that the scaling down of memory technology is faced with the limitations of the optical-lithography process,[39] various kinds of strategies, such as the engineering of structures, materials, and interfaces, have been suggested for the reduction of the high writing reset current.[46–51]

A recent study on switching power reduction of PCM has been demonstrated by incorporation of self-assembled BCP nanostructures.[7] Park et al.[7] reported that SiO_x nanostructures (dots, lines, and perforated lamellae) produced by a combined process of BCP self-assembly of Si-containing PS-*b*-PDMS with follow-up reactive ion etching (oxygen plasma etching) was used to regulate the contact area between a GST film and a TiN heater electrode, thus demonstrating noticeable reductions of the reset current and the switching power. The use of PS-*b*-PDMS was strongly motivated by the fact that the spatial arrangement of tunable SiO_x nanostructures enables a comparison of four different contact areas directly related to the device performance metrics (**Figure 2**a). The scanning electron microscopy (SEM) image in Figure 2b shows a cross-sectional view of self-assembled SiO_x nanostructures within the circular hole of a PCM device. As mentioned above, various shapes of SiO_x nanostructures converted from PDMS domains, including small spheres, large spheres, parallel cylinders, and hexagonally perforated lamellae (HPL), were produced by changing

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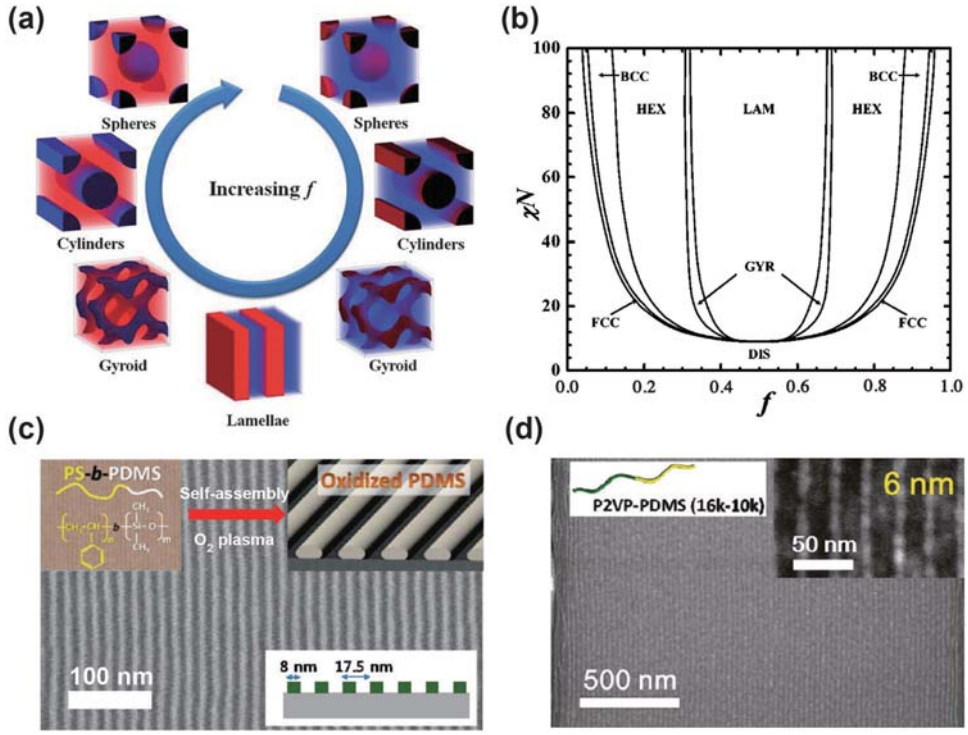

Figure 1. a) A variety of nanostructures generated by BCP self-assembly. Here, *f* denotes the volume fraction of one component. b) Theoretical phase diagram of diblocks predicted by the self-consistent mean-field theory, depending on the volume fraction (*f*) of the blocks and the segregation parameter, χN, where χ is the Flory–Huggins segment–segment interaction energy and *N* denotes the degree of polymerization. BCC, LAM, and HEX indicate spherical, lamellar, and cylindrical morphologies, respectively. c) Monolayer of cylinders of (17.5 nm period/8 nm line width) PS-*b*-PDMS. The insets show sketches of the structure of the PS-PDMS BCP and a schematic view of the oxidized PDMS cylinders after oxygen etching. d) 6 nm linewidth pattern using P2VP-PDMS as a BCP. The inset shows a magnified SEM image. a,b) Reproduced with permission.[26] Copyright 2013, RSC Publishing. c) Reproduced with permission.[27] Copyright 2010, American Chemical Society. d) Reproduced with permission.[28] Copyright 2011, American Chemical Society.

the molecular weight (MW) of BCPs and the solvent treatment time,[52,53] thereby resulting in a change of the fill factor (FF), as shown in Figure 2c–f. The FF can be defined as the occupied area ratio of SiO_x nanostructures on GST film; accordingly, the contact area between GST and TiN can be decreased as the FF increases. It is noteworthy that a decrease in the contact area between GST and TiN expectedly triggers a reduction of the reset current. Both the reset current and the switching power decreased as the fill factor increased (Figure 2g,h). These observations directly reflect that the areal fraction of the crystalline phase of GST film can be controlled by tuning the equilibrium morphology of self-assembled SiO_x nanostructures, which affects the variation of the reset current and the switching power. While previous DSA approaches have mostly focused on scaling down,[54] the BCP self-assembly strategy in this PCM device provides a new potential approach for modulating the contact area in practical devices beyond scaling down.

There has been strong demand for flexible non-volatile memory in order to realize system-on-plastic (SoP) devices, as these devices are expected to play an important role in flexible electronics applications, including data storage, computing processing, and communication with other electronic devices.[55,56] A significant limitation with regard to the use of flexible PCM devices is caused by the high reset current of PCM devices, which induces serious failure during writing/erasing operations on flexible substrates. As mentioned above, although a variety of approaches have been proposed to reduce the reset current,[46–51] it is difficult to to apply these methods on plastic substrates owing to the temperature limit. Furthermore, advanced high-resolution lithography techniques such as double-patterning technology (DPT) and e-beam lithography cannot easily be applied to rough plastic substrates because high-precision focusing is required.[57] Although some previous studies have reportedly demonstrated flexible PCM, most of the resulting devices use nanowire and nanodot arrays,[58,59] making them unfeasible solutions for the commercialization of flexible phase-change random access memory (PRAM) due to their incompatibility with high-density interconnections. To overcome these issues, Mun et al.[36] developed a flexible PCM device that relied on the use of the self-assembled BCP nanodomains for next-generation non-volatile memory applications. **Figure 3**a shows a schematic illustration of the flexible PCM arrays on a plastic substrate. As in the above-mentioned study, self-assembled SiO_x nanostructures were inserted into a 2 μm contact hole in an effort to decrease the contact area between the GST film and the TiN heater electrode, as the reset current of a conventional PCM device with a 2 μm contact hole is very high (ca. 58 mA) when used in flexible memory applications. This type of conceptual flexible PCM device was fabricated on a 25 μm-thick polyimide (PI) film (Figure 3b). Intriguingly, no cracking or

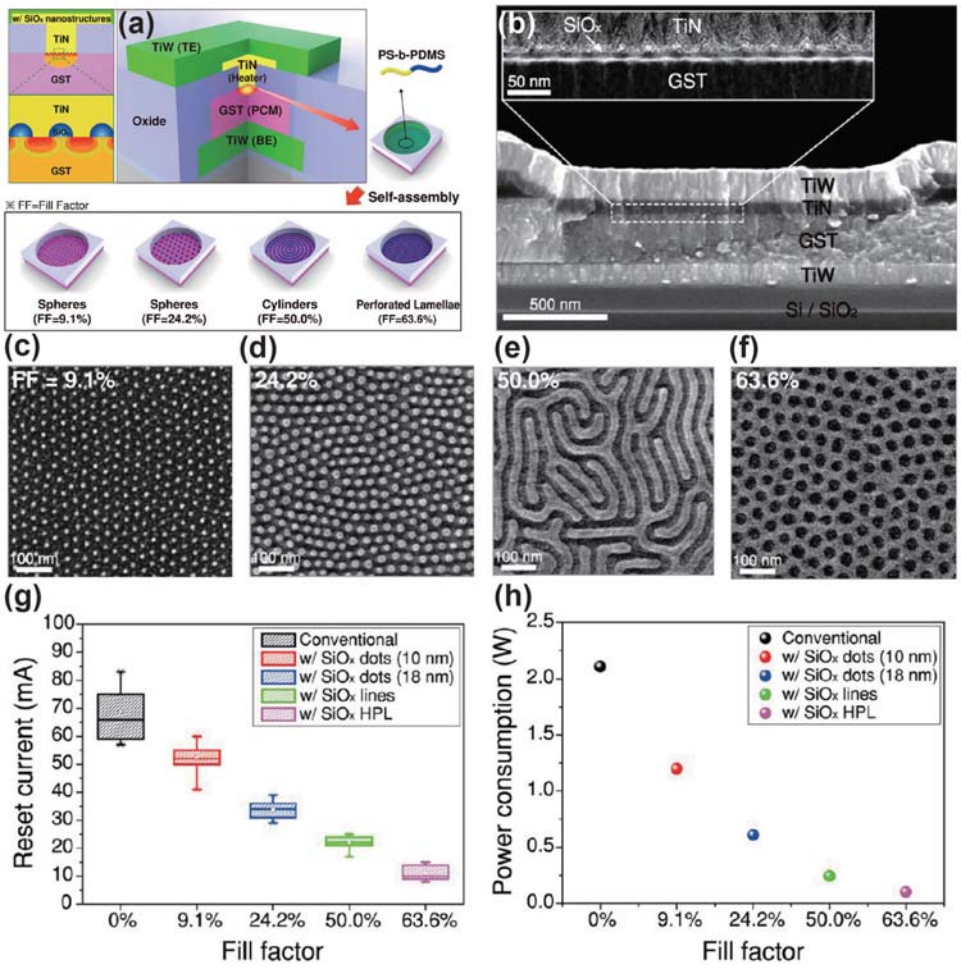

Figure 2. a) Schematic of the PCM device structure. The lower inset shows that various morphologies of the self-assembled nanostructures between GST and TiN. b) Cross-sectional SEM images of a PCM device. The inset shows a TEM image of the interface between TiN and GST, where the self-assembled nanostructures are inserted. c–f) SEM images of the self-assembled nanostructures formed on GST thin films: small spheres (FF = 9.1%) (c), large spheres (24.2%) (d), cylinders (50.0%) (e), and hexagonally perforated lamellae (HPL) (63.6%) (f). g) Reset current trend with an increase in the FF, indicating a proportional decrease of the writing current with an increase in the FF. h) Power consumption trend with increasing fill factor. a–h) Reproduced with permission.[7] Copyright 2013, American Chemical Society.

deformation was observed when the device was rolled on a glass rod as shown in the inset of Figure 3b. The cross-sectional SEM image of a flexible BCP-incorporated PCM (f-BPCM) examines the spatial-integration of silicon oxide nanopatterns between the GST phase-change material and a TiN heater electrode (Figure 3c). These flattened cylindrical SiO_x morphologies were utilized to reduce the contact area and decrease the reset current during writing operations. In these flexible PCM arrays, the PCM unit cell consisted of the f-BPCM based on GST and a single-crystal silicon diode as a selection element. By integrating high-performance silicon diodes with f-BPCM devices, the memory operation of the 1D–1P unit cell was successfully demonstrated for the application of the flexible PRAM.[55,56] The resistance–voltage (*R*–*V*) characteristics of the flexible 1D–1P unit cell at a forward/reverse pulse voltage showed excellent switching between the crystalline and the amorphous states in forward bias with a resistance ratio of 20, whereas there was no switching behavior at reverse bias due to the rectifying property of the selection device. The current–voltage (*I*–*V*) characteristics of the flexible 1D–1P unit cell shown in the inset of Figure 3d also support the fact that resistance switching was only observed under forward bias. The experimental measurements demonstrated that the coupling of the f-BPCM with a flexible Si diode plays a critical role in diminishing cell-to-cell interference without operating error. To confirm the mechanical reliability of the 1D–1P device, the bending tests were carried out as a function of the bending radius (Figure 3e) and the number of bending cycles (Figure 3f). From these results, the flexible 1D–1P device was shown to be highly stable under flexed conditions, which is directly related to its compatibility with flexible electronic applications. This work has provided a useful approach to attain flexible PRAM to overcome the high reset current issue through BCP patterning.

2.2. RRAM Devices

Resistive random access memory (RRAM) has attracted much attention as a promising alternative for future non-volatile

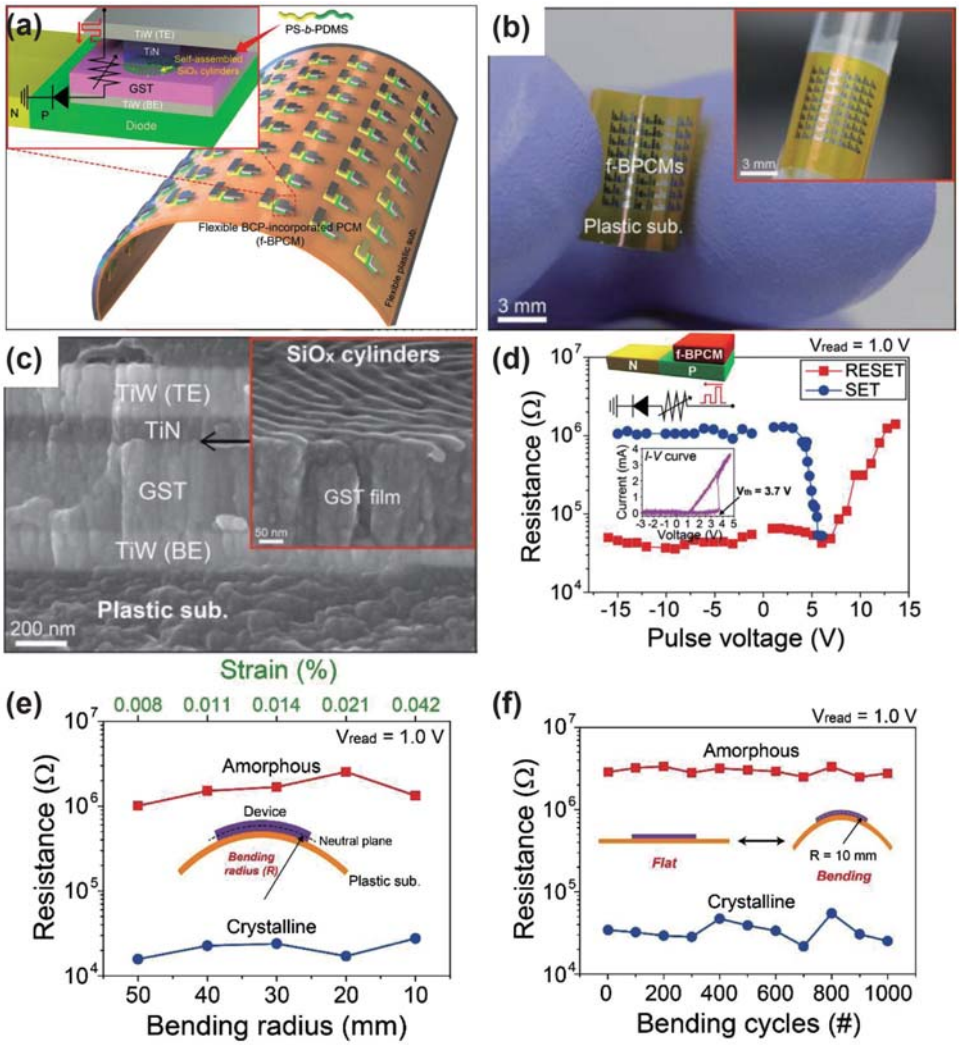

Figure 3. a) Schematic of f-BPCM arrays with diodes on a plastic substrate. The inset image shows a device structure integrated with a single silicon diode and the PCM inserted into SiO_x nanostructures. b) Photograph of the f-BPCM cells with diodes on a 25 μm-thick polyimide substrate. The inset shows the device wrapped around a glass rod with a diameter of 7 mm. c) Cross-sectional SEM image of the f-BPCM device. The inset shows a tilted SEM image of self-assembled SiO_x nanostructures on GST thin films. d) *R–V* curves of a flexible 1D–1P unit cell at a forward/reverse pulse voltage and the corresponding circuit diagram. The inset graph shows the *I–V* curves of a 1D–1P unit cell on a plastic substrate. The pulse widths for SET (solid blue circle) and RESET (solid red square) operations were set to be 1 μs and 140 ns, respectively. e) Resistance ratio between the amorphous and crystalline states and strain in GST films as a function of the bending radius. f) Resistance ratio of the device during the 1000 repeated bending cycles with a 10 mm-bending radius. a–f) Reproduced with permission.[36] Copyright 2015, American Chemical Society.

memory due to its potential advantages, such as its high storage density with 3D packing, fast switching speeds, low energy consumption, low processing temperatures, and good compatibility with the existing CMOS process.[43,60–62] RRAM devices typically exhibit two resistance states: a high resistance state (HRS) and a low resistance state (LRS). The resistance switching from the HRS to the LRS is defined as a SET process, whereas switching operation from LRS to HRS is a RESET process.[63] On the basis of the voltage polarity of SET and RESET operations, two resistive-switching schemes of unipolar and bipolar switching have been reported.[62–65] Unipolar resistive switching memory does not depend on the voltage polarity for the SET and RESET processes,[56,60,66,67] whereas a bipolar switching device relies on the voltage polarity to change its resistance states (i.e., V_{Reset} and V_{set} have opposite polarities).[43,55] Despite the fact that bipolar RRAM possibly allows better switching stability than unipolar RRAM, the unipolar switching mode based on Cu_xO,[56] NiO,[66] ZnO,[67] and TiO_2[60] is likely preferred for high-density memory applications due to its excellent compatibility with two-terminal stackable selector elements.[60,66,68] Notably, the unipolar switching mechanism has been well defined in relation to the generation and rupture of conductive filaments (CFs) in the oxide layer.[63–65] There has been significant concern over the random formation and rupture of CFs, which could give rise to both a large distribution of the SET/RESET voltage and wide fluctuation of the resistance ratio between the HRS and the LRS (i.e., device uniformity and reliability),[69–71] thereby

restricting the practical application as a next-generation non-volatile memory. To settle the reliability and uniformity issues, various solutions have been suggested, including the insertion of an interface layer,[69] a change of the crystal structure,[72] doping,[73] and the incorporation of metal nanoparticles,[70] for the purpose of controlling the generation and rupture of CFs during memory operations.

In a recent study, it was reported that the reliability of a unipolar resistive switching device can apparently be enhanced via the self-assembly of BCPs.[8] In this work, the formation and rupture of CFs was highly regulated by uniformly distributed SiO_x nanodots (SiO_x-NDs) which were created by the self-assembly of Si-containing PS-*b*-PDMS over the interfacial areas between a resistive-change material (NiO) and a Pt/Ti top electrode, thus leading to a narrow distribution of the SET/RESET voltage and less fluctuation of the resistance uniformity. **Figure 4**a shows a schematic illustration of the device structure developed in this work. A metal–insulator–metal (MIM) structure consisting of Pt/Ti/plasma-oxidized NiO/Ni and the spatial positioning of SiO_x-NDs on the NiO layer was verified by scanning electron microscopy (SEM) (Figure 4b and the upper inset) and transmission electron microscopy (TEM) (lower inset). It is noteworthy that hexagonally ordered SiO_x-NDs were obtained by the plasma etching of the self-assembled PDMS spheres upon the solvent-vapor annealing of the Si-containing PS-*b*-PDMS BCP.

To compare the performance enhancement between a conventional memory cell without SiO_x-NDs and a memory cell with SiO_x-NDs, the electrical properties were evaluated in direct current (DC) sweep mode by applying repeated voltage sweeps. As shown in Figure 4c and d, the uniformity and reliability of the memory cell with the SiO_x-NDs was significantly improved compared with memory cell without SiO_x-NDs. High-resolution transmission electron microscopy (HRTEM) images confirmed the controlled formation of CFs in the NiO layer as induced by the self-assembled SiO_x-NDs during the RESET/SET process. Cone-shaped Ni filaments (the yellow dotted triangles) with a different contrast background were observed on the NiO layer. Ni filaments were separated from the top electrode of Pt/Ti at the HRS (Figure 4e), while connection of the filaments with thin Ti films was detected at the LRS. This observation clearly indicates that the metallic Ni filaments served as current paths inside the NiO films and that the SiO_x-NDs played a crucial role in confining the location where the CFs were generated, thus ultimately resulting in an enhancement of the uniformity of unipolar NiO resistive memory. The directed self-assembly of Si-containing BCPs can be further exploited to design and fabricate unipolar resistive memory devices.[7]

2.3. Nanocrystal Charge-Trap Flash Memory Devices

Recently, since the demand for NAND (NOT AND) floating-gate-type flash memory is growing rapidly with the development of mobile and portable electronic devices, such memory devices have gained an enormous market potential due to the high storage capacity, high memory retention rates, and low cost.[74] Particularly, in order to manufacture smaller and thinner NAND flash memory, the device dimensions should be aggressively scaled down to the sub-10 nm range.[75] However, further thinning of the tunneling oxide resulting from these down-scaling efforts is potentially accompanied by an undesired increase in the cell-to-cell interference and leakage issue (i.e., the direct-tunneling of stored charge carriers).[76,77] Accordingly, a new conceptual approach using spatially ordered nanocrystal (NC) arrays as charge-storage layers has been studied,[78–83] envisaging a promising route for the replacement of conventional film-type floating-gate flash-memory devices. In NC charge-trap memory, the charge carriers are trapped in the NC by applying a programming pulse. The charge-trap density and distribution can be readily controlled by the spatial positioning of the NCs, thereby giving rise to excellent endurance, a high chip density, superior reliability, and low power consumption.[76] Since Tiwari et al.[83] realized improved performance in a flash-memory device using Si NCs for the first time, a number of studies have been reported using various semiconducting and metallic NCs materials as charge-storage layers.[84–87] Because metallic NCs have a high density of states at the Fermi level, electrons can be stored more in metallic NCs, thus enabling the production of a wide memory window of the type required for multilevel states in one unit cell. Among the many methods of forming metallic NCs within the charge-trapping layer, BCP self-assembly is now regarded as being the strongest candidate due to its straightforward control over the morphological shapes and geometrical dimensions, which have strong influences on controlling the density, distribution, and ordering of metal NCs at a low temperature.[34,88]

Lee et al.[34] reported the fabrication of non-volatile NC charge-trap flash memory using spatially defined cobalt NCs obtained by the self-assembly of a micelle-forming diblock copolymer. **Figure 5**a schematically illustrates the entire fabrication procedure of the NC charge-trap flash-memory device. First, HfO_2 tunneling oxide layers were grown on a p-type Si substrate by using a radio-frequency magnetron sputtering system. After that, cobalt NCs were formed on the tunneling oxide using a polystyrene-*block*-poly(4-vinylpyridine) (PS-*b*-PVP). A $CoCl_2 \cdot xH_2O$ precursor was put into a 0.5 wt% toluene solution of the PS-*b*-PVP micelles. A monolayer film of PS-*b*-PVP micelles with $CoCl_2 \cdot xH_2O$ in the PVP core was then formed by spin-coating. This single-layered film was treated with O_2 plasma to synthesize cobalt oxide nanoparticles and then the resulting cobalt oxide nanoparticles were reduced by means of H_2 annealing at 300 °C. To form the blocking oxide layer, a 15-nm-thick HfO_2 layer was deposited using a sputtering system, and Pt gate electrodes were patterned using a conventional lift-off process. Figure 5b shows an SEM image of the reduced cobalt NC array on the HfO_2 tunneling oxide. The average NC size and density were measured to be 10.5 ± 1.7 nm and 1.3×10^{11} cm^{-2}, respectively. To evaluate the electrical characteristics of the formation of the metallic cobalt NC array, capacitance–voltage (*C*–*V*) measurements were performed (Figure 5c). The memory window, which is defined as the difference in the threshold voltages between the programmed and the erased states, was observed to be widened from 0.65 to 1.49 V when the cobalt oxide NCs were reduced to metallic cobalt. This study demonstrated that NC charge-trap-type flash-memory devices could be fabricated using self-assembled diblock-copolymer micelles as an NC template.

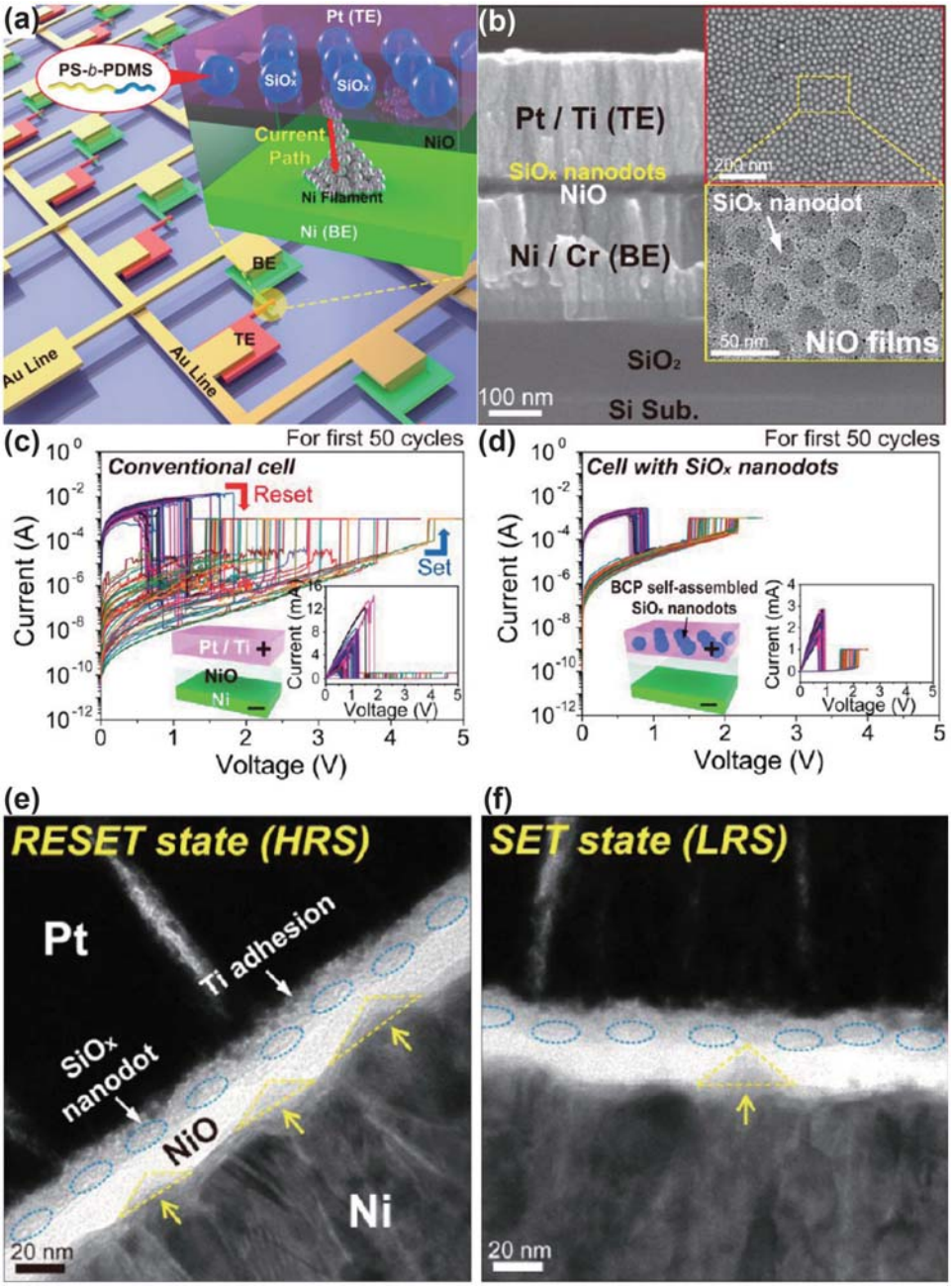

Figure 4. a) Schematic of NiO resistive memory with self-assembled SiO_x-NDs and the switching mechanism by Ni CFs. The NiO memory consists of Pt (top electrode), NiO (resistive material), and Ni (bottom electrode). Self-assembled SiO_x-NDs are introduced by the solvent annealing and plasma etching of Si-containing PS-*b*-PDMS BCPs. b) Cross-sectional SEM image of Ni/NiO/Ti/Pt resistive memory with self-assembled SiO_x-NDs. The top view SEM and TEM images indicate hexagonally formed SiO_x-NDs on NiO films. c,d) SET and RESET voltage distributions of NiO resistive memory devices without/with self-assembled SiO_x-NDs. *I–V* curves obtained from the NiO memory devices while the switching for 50 cycles: without self-assembled SiO_x-NDs (conventional cell) (c) and with self-assembled SiO_x-NDs (d). The insets exhibit their linear *I–V* curves. e,f) TEM image analyses obtained from NiO memory devices with self-assembled SiO_x-NDs for the observation of CFs. TEM images of a device: after a RESET operation (HRS) (e), and after a SET operation (LRS) (f). The blue dotted circles indicate the SiO_x-NDs, and the yellow dotted triangles represent the Ni CFs. a–f) Reproduced with permission.[8] Copyright 2014, American Chemical Society.

Thus far, there have been several reports of the use of metal NCs that are formed by BCP self-assembly for charge-storage flash-memory devices.[89,90] These studies revealed that the key parameters are the density and species of the metallic NCs for the realization of MLC (multi-level cell) and TLC (triple-level cell) devices (or more), as these factors determine the number of stored charge carriers in the memory unit cell under the same memory operation condition, which is associated with the memory window. Shin et al.[35] recently developed multi-component nanopatterns by directed BCP self-assembly. In

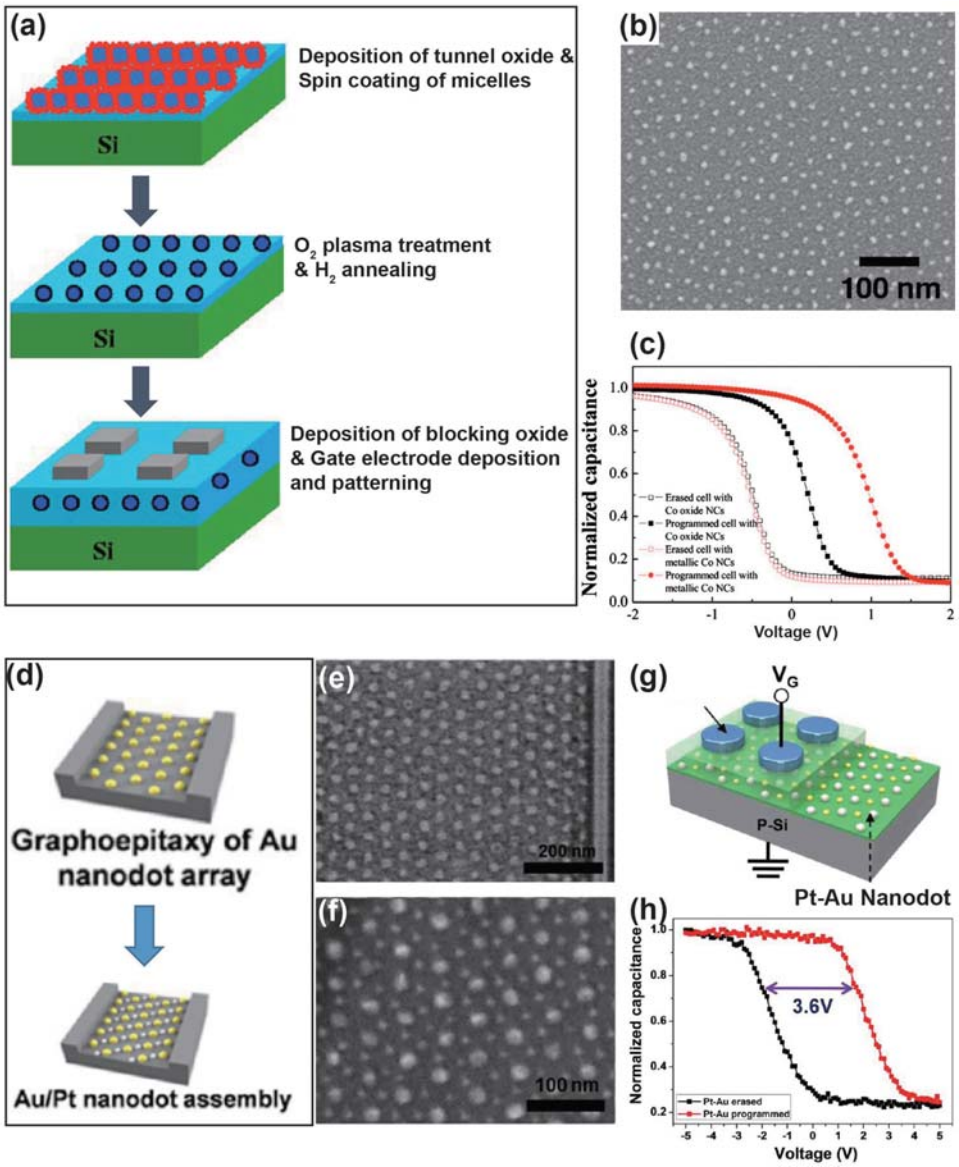

Figure 5. a) Schematic illustration of the device fabrication procedures. b) Metallic Co NC array reduced by H_2 annealing. c) *C–V* curves of the memory devices with Co oxide and metallic Co NCs. *C–V* curves measured after the application of program/erase bias pulses. d) Schematic procedure of multicomponent nanopatterning. e) Au nanodot array. f) Au–Pt nanodot array. g) Device structure of a charge-trap memory device. h) *C–V* curves of the devices with Pt–Au binary nanodot arrays. *C–V* curves obtained from programmed and erased states a–c). Reproduced with permission.[34] Copyright 2007, AIP Publishing. d–h) Reproduced with permission.[35] Copyright 2013, American Chemical Society.

general, self-assembled BCP thin films are composed of single-shaped nanodomains such as cylinders, lamellae, or spheres, as it is difficult to integrate two or more nanodomains. In this work, multicomponent nanopatterns were adopted to overcome the limit of charge-trap memory for large-area scalability, enabling an increased memory window in flash memory and, thus, the realization of multilevel NAND flash memory. Figure 5d shows a representative schematic illustration of directed self-assembly by a two-step process. The first self-assembly step for the formation of hexagonal Au nanodot arrays was directed by the graphoepitaxy effect from topographically prepatterned substrates (Figure 5e). The graphoepitaxy effect of BCP is used as a scalable and highly ordered nanostructure for improving the memory window of electronic application.[91–93] The second self-assembly of the overlaid PS-*b*-P4VP thin films contained the bottom Au nanodot arrays, and final pattern transfer by metallization produced graphoepitaxially ordered multicomponent nanopatterns of a Pt–Au binary nanodot array (Figure 5f). Platinum and gold are preferred as metallic NC materials owing to their high work functions, thus they induce the formation of a deep potential-well depth to store more charge carriers in NCs of the same size and density.[76,94,95] Figure 5g schematically illustrates the device structure of flash memory, which uses Pt–Au nanodot arrays as a charge-trapping site. The *C–V* characteristics were measured to estimate the variation in threshold voltage by applying bias pulses of 7 V/50 ms (program) and

–13 V/30 ms (erase), as shown in Figure 5h. In comparison with a Pt or Au single-nanodot array, a flash-memory device with a Pt–Au binary nanodot exhibited a wider memory window of 3.6 V due to an increase in its charge-trap density. This work demonstrated that the memory window could be increased by employing a multicomponent nanopattern combination. The research approach based on the BCP self-assembly technique is one of the strongest tools for the realization of metallic NC charge-trap flash memory, providing novel solutions for controlling the metal species, size, and density.

3. Electrical Sensor Devices

The electrical detection of target species such as gas and biological molecules is one of the emerging research topics in the field of nanotechnology.[4,96] Electric field-effect transistor (FET) types of sensors provide an attractive platform on which to sense the contents of biological or gas species due to the direct conversion of target samples to electronic signals, thus allowing more-convenient and rapid detection.[96,97] Nanostructured channels in electric FET type sensors have been intensively investigated for electrical sensing, as the dimensional features of the nanostructured channel are comparable to the scale of gas and biological species.[4,96,98–103] The fabrication route for nanostructured channels can be categorized into two representative types: top-down and bottom-up.[104–106] In the top-down approach, the position and uniformity of the nanostructured channels are mainly governed by the resolution limit of the conventional photolithography process.[106] As stated in the introduction, e-beam lithography still has drawbacks when attempting to create nanostructured channels over large areas at a low cost.[21] As an alternative, bottom-up BCP self-assembly patterning is currently considered as a promising means of producing spatially ordered nanostructures on a wide nanometer scale, confirming the precise control over the geometrical features.[24,28]

Jung et al.[23] reported an electrical gas sensor that employed highly ordered conductive polymer nanowires enabled by bottom-up BCP self-assembly. **Figure 6**a shows a schematic illustration describing the device structure made from the multi-positioning of conductive polymer nanowires. To fabricate polymer nanowires, poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS), SiO_2, and poly(dimethylsiloxane) (PDMS) monopolymer brush were formed in sequence on a silica-coated silicon substrate with 1.3 μm trenches. Afterward, flattened PDMS cylinders were self-assembled in a PS matrix within the trenches, utilizing PS-*b*-PDMS BCP. Using the array of PDMS cylinders as an etching mask, PEDOT:PSS nanowires were produced through a reactive ion etching processes. The patterned PEDOT:PSS nanowires, with a 15 nm width and a 20 nm height, are shown in Figure 6b. To verify the potential application of conductive polymer nanowires, a two-terminal gas sensor was fabricated using PEDOT:PSS nanowires as a conductive channel for the sensing of a target vapor. Figure 6c displays the resistance change of the conductive polymer nanowires while varying the ethanol concentrations in the N_2 as a carrier gas. The normalized resistance of the device was observed to be increased with the partial pressure of ethanol, confirming the capability of this gas sensor to detect ethanol vapor. This work showed that it was possible to detect target vapor through a conductive nanowire fabricated by BCP self-assembly.

Recently, Jeong et al.[9] demonstrated the electrical detection of biomolecules on a nanopatterned silicon surface fabricated by the bottom-up BCP self-assembly process. Figure 6d illustrates schematically an FET-type biosensor functionalized with biotin molecules for sensing avidin or streptavidin proteins. To optimize the sensitivity of the device, a Si nanomesh channel patterned by BCP lithography was selected. Vertical hexagonal cylinder arrays of a polystyrene-*block*-poly(methyl methacrylate) (PS-*b*-PMMA) thin film were used as a template for generating Si nanomesh structures with sub-20 nm features. A patterned nanomesh of a p-type Si channel with a diameter of 15 nm was observed by cross-sectional SEM after the pattern-transfer process. This nanostructured channel was thin enough for the detection of target biomolecules because the dimensional scale of the resulting nanomesh was comparable to the Debye screening length.[107] To assess the capability of detecting streptavidin and avidin proteins electrically, the biosensor device was used to measure various target biomolecular proteins and related concentrations in a phosphate-buffered saline (PBS) (pH 7.4) solution, as shown in Figure 6f. These variations were reportedly attributed to the hole accumulation (Figure 6f(i)) and depletion (Figure 6f(ii)) induced by the polarity of the charged biomolecule, thereby changing the potential barrier in the nanomesh p-type silicon channel.[96] This patterning process based on BCP self-assembly has the merits of being highly scalable with a high throughput. Therefore, the BCP patterning technique can offer the possibility of fabricating highly sensitive electric sensor devices at a low cost.

4. Energy Devices for Self-Powered Application

4.1. Triboelectric Nanogenerator (TENG) Devices

Developing self-powered flexible electronic systems is of great importance for wearable and implanted biomedical devices.[108–112] In particular, mechanical energy-harvesting systems using nanogenerators have attracted a considerable amount of research attention due to the technological possibility of realizing self-powered electronic systems.[113] Several relevant studies have been performed based on piezoelectric devices,[114–116] electromagnetic induction,[117] and triboelectric effects.[118–121] Among them, triboelectric nanogenerators (TENGs) are especially promising owing their high output power and cost-effective simple process.[122,123]

The operation principle of the TENG is based on a combination of the triboelectric effect and the electrostatic induction.[108] If two materials that exhibit opposite tribo-polarity come into mechanical contact, a charge transfer takes place at their interface.[108,124] When the two materials separate, the electrostatic potential difference induced by the oppositely charged surfaces enables the generation of a current flow through an external load.[125] To date, performance enhancements of the output power of TENGs are an important task for practical applications. In this light, many studies have been carried out using a variety of TENG concepts, including surface-linked

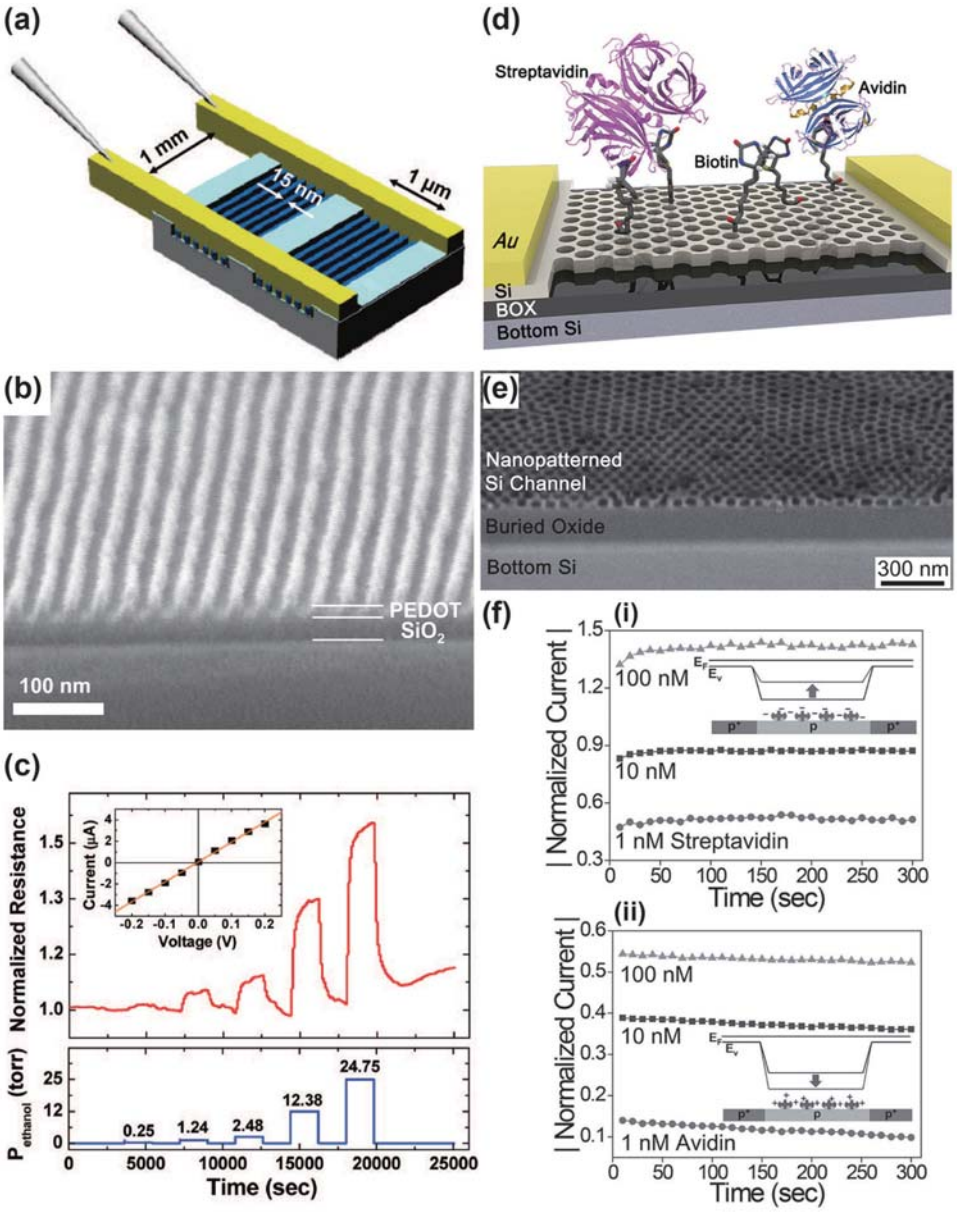

Figure 6. a) Schematic illustration of a vapor detector based on PEDOT:PSS nanowires. 50 nm-thick Au electrodes, 1 mm apart, are formed perpendicular to the nanowires. b) The SEM image shows PEDOT:PSS nanowires formed by O_2/H_2 reactive ion etching. c) The resistance variation of the polymer nanowires as a function of the concentrations of ethanol vapor. d) An FET-based nanomesh patterned biosensor functionalized with biotin molecules for detecting streptavidin or avidin protein (BOX = buried oxide). e) Cross-sectional SEM image of the nanopatterned top silicon layer (ca. 25 nm thickness). f) Current variations upon streptavidin (i) and avidin (ii) binding at the nanopatterned channel. The insets indicate the change of the valence band state of the channel after streptavidin and avidin binding. a–c) Reproduced with permission.[23] Copyright 2008, American Chemical Society. d–f) Reproduced with permission.[9] Copyright 2014, John Wiley & Sons.

nanoparticles,[126] innovative device structures,[121,125–133] polymer dry-etching,[134] and various surface morphologies[135–139] in an effort to increase the surface contact area. Although numerous research groups have suggested various approaches for modifying the surface morphologies on the nanometer scale for the purpose of improving the output power of TENGs, significant limitations remain, such as poor controllability, restricted material selection, lack of topological order, and irrevocable morphologies.[121,126,134–139] To improve the performance of TENGs further, BCP self-assembly has emerged as an alternative method to achieve tunable nanoscale patterns based on rings, holes, lines, and dots.[52,140–143]

To demonstrate the robustness of the directed BCP self-assembly process as a surface-modification technique, Jeong et al.[10] investigated a topographically designed triboelectric nanogenerator using the self-assembly Si-containing PS-*b*-PDMS. **Figure 7**a schematically illustrates the fabrication procedures used to create nanopatterned TENGs through BCP

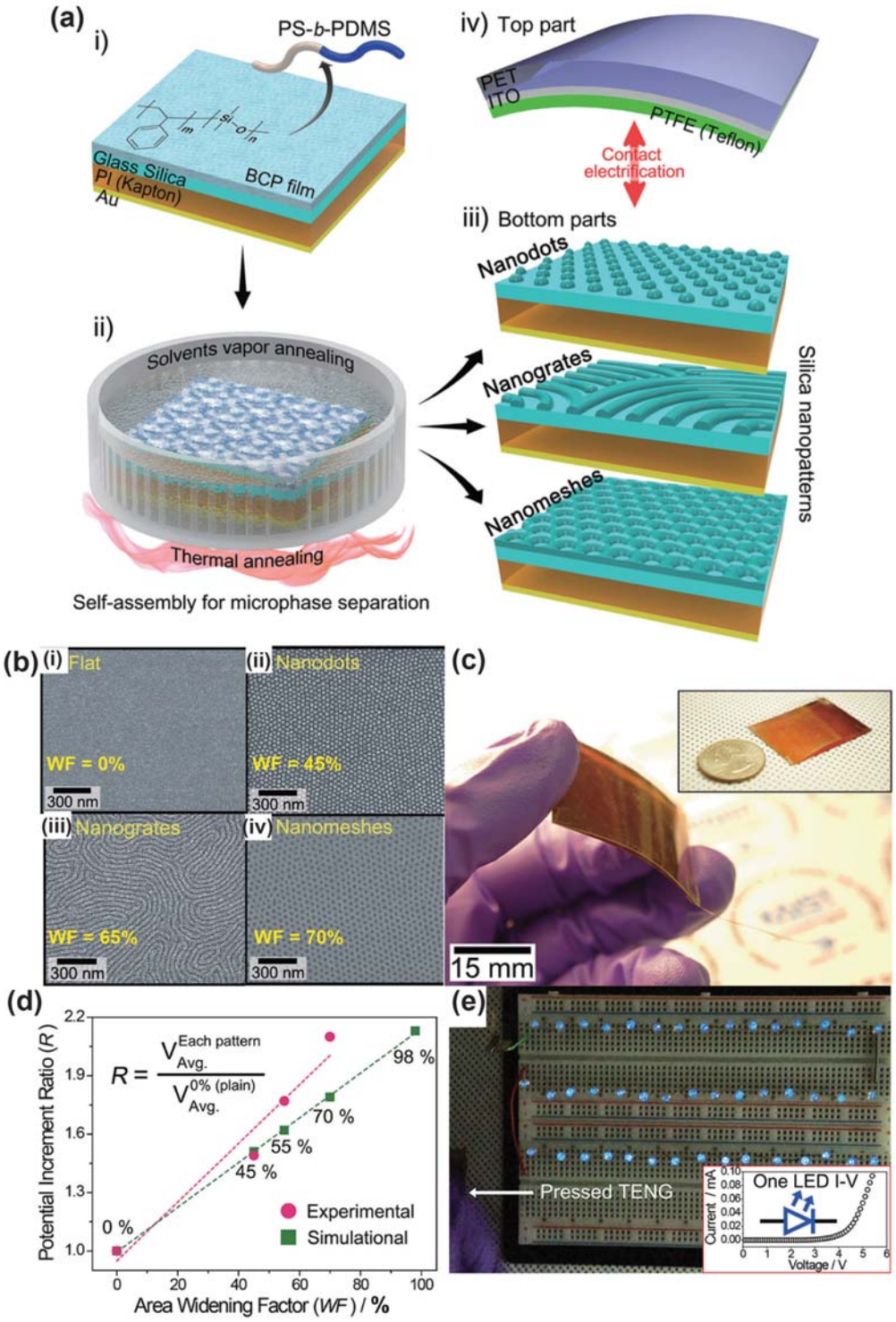

Figure 7. a) The schematic illustration of the BCP-TENGs. i) Spin-casting of PS-*b*-PDMS BCP solutions onto an Au/Kapton PI/glass silica substrate. ii) Thermal and solvent vapor annealing for the microphase separation of BCP films. iii) Different types of silica nanopatterns obtained from the tunable BCP self-assembly to produce bottom parts of diverse BCP-TENGs. iv) The arch-shaped top part (Teflon PTFE/ITO/PET) for contact electrification. b) SEM images of various surface morphologies for use in bottom parts. i) flat TENG; ii) nanodot BCP-TENG; iii) nanograte BCP-TENG; iv) nanomeshBCP-TENG. c) Photographic images of an as-fabricated BCP-TENG device. d) Electric potential versus the area WF (related to nanopatterning) in the experimental and simulation data. In the experiments, the nanomeshBCP-TENG (WF = 70%) provided the highest electrical output. e) The instantaneous lighting-up of 45 blue LEDs in series when the nanomesh BCP-TENG was pressed by a human finger without any external energy source. The inset indicates the turn-on voltage of one blue LED (ca. 3 V) in the *I–V* curve. a–d) Reproduced with permission.[10] Copyright 2014, American Chemical Society.

self-assembly. The BCP-TENG has two parts, a top part and a bottom part. The bottom part consists of an Au bottom electrode, a polyimide (PI) substrate, and glass silica (Figure 7a(i)), while the top part is composed of a polytetrafluoroethylene (PTFE)-based thin film and an indium tin oxide (ITO)-coated poly(ethylene terephthalate) (PET) substrate (Figure 7a(iv)). The gap distance between the top and bottom parts was measured to be ca. 2 mm, which is widely considered to be the optimized distance for the high output power from a TENG device.[144] In this work, the choice of PS-*b*-PDMS as a topologically controllable soft surface was motivated by the fact that the PDMS blocks in a self-assembled Si-containing PS-*b*-PDMS BCP can easily be converted into silica nanostructures utilizing CF_4/O_2 plasma treatment.[145] To check the performance enhancement depending on the surface morphology, spheres (nanodots), fingerprint-like cylinders (nanograts), and gyroid-based HPL (nanomeshes) devices were used to generate three types of silica nanostructures with three categories of PS-*b*-PDMS BCPs. The widening factor (WF) is defined as the increase in the surface area ratio when compared to a flat surface, the WFs of nanodots, nanograts, and nanomeshes were 45%, 55%, and 70%, respectively (Figure 7b). The BCP-TENG device was fabricated using flexible PI and PET substrates, for use in self-powered flexible electronic systems as an energy source (Figure 7c). To extract the output power and WF relationships, the potential increment ratio (*R*) was utilized to compare performance variations as a function of the WF (Figure 7d). Clearly, the potential increment ratio was gradually improved with an increasing area-widening factor. This experimental observation indicated that the surface nano-morphology has a strong influence on the output voltage of a BCP-TENGs. As a practical demonstration, 45 blue LEDs were instantaneously turned on using a BCP-TENG with nanomeshes by the tapping of a hand (Figure 7e). This work demonstrates a robust strategy to realize high-performance TENG devices via surface morphology modifications through BCP self-assembly. The self-assembled BCP TENG is an interesting research topic for achieving optimum energy harvesting, enabling the use of various triboelectric modes,[146–148] diverse device architectures,[129–131,133] and multilayered integration methods.[149,150]

4.2. Dye-Sensitized Solar Cell (DSSC) Devices

Solid-state dye-sensitized solar cells (DSSCs) have received much attention as a next-generation solar cell due to their potential to replace conventional silicon-based solar cells.[151–154] Generally, a DSSC consists of a dye-assembled TiO_2 layer, a liquid or solid electrolyte, and a counter electrode. These layers are surrounded by conductive glass substrates.[152–155] Since the dyes play major roles in absorbing light and separating the charges in DSSCs,[156] the formation of a nanostructured TiO_2 thin film with a high surface-area-to-volume ratio is crucial because it increases the number of dyes chemically attached to the TiO_2 film.[157,158] There have been several reports of the use of sol–gel-processed sintered nanoparticles;[156,159–161] these approaches are strongly competitive for creating highly ordered and porous films. The BCP self-assembly process is generally accepted as a promising means of controlling the morphology of the TiO_2 nanostructures. This technique enables the creation of well-ordered nanostructures over high surface areas for further improvements of DSSCs.[12,162,163] Nedelcu et al.[163] reported the role of the morphology and crystallinity of mesoporous TiO_2 with PI-*b*-PEO BCP self-assembly in a solid-state DSSC. This work revealed that higher power conversion efficiencies could be achieved with larger open-pore structures, as derived from the improved dye loading and invasion by a the hole-transporter.

Studies reported by Nedelcu et al.[163] and Docampo et al.[37] placed more emphasis on the crystallization environment of mesoporous TiO_2 and its effect on the DSSC performance while utilizing diblock copolymer PI-*b*-PEO. To evaluate the influence of the crystallization environment on the DSSC device performance, three titania hybrid composites were prepared by changing the ratio between the titania and the polymer used. **Figure 8**a schematically illustrates the whole fabrication process of the sol–gel self-assembly, and three morphologies are presented, i.e., TiO_2-rich cylinders in an organic matrix (titania 1:3), organic cylinders in a TiO_2-rich matrix (titania 2:1), and organic micelles in a TiO_2-rich matrix (titania 1:1). Figures 8b(i)–(vi) show transmission electron microscopy (TEM) images that describe the hybrid materials for the three recipes before and after calcination. In this work, it was found that different morphologies affected the local environment for the crystallization of TiO_2. Therefore, it is strongly predicted that the electronic structure of TiO_2 can be readily governed by the morphology. Figure 8c shows the current-density–voltage (*J*–*V*) curves of the devices fabricated with three different morphologies; the "S" curve was acquired from a reference cell fabricated by a standard nanoparticle process. Among the three devices, the titania 1:3 device exhibited the highest short-circuit current of 7.5 mA cm^{-2} as well as the best power conversion efficiency of 3.2%. These results were comparable to those of a standard nanoparticle-based device. This study indicated that it was possible to alter the distribution of the electronic sub-bandgap states by modifying the morphology of the TiO_2 by means of diblock copolymer self-assembly.

In a DSSC device, it is well known that achieving continuous connectivity of all electronically active phases to the device electrode is particular challenging using BCP self-assembly because most copolymer morphologies, such as lamellae or columns, are continuous in one dimension. This usually needs additional processing steps to control the orientation of the nanostructure.[12] To overcome this issue, a diblock copolymer with a cubic bicontinuous double-gyroid morphology was introduced. Crossland et al. examined the use of a BCP-based bicontinuous cubic double-gyroid anatase TiO_2 morphology in DSSCs.[38] Figure 8d shows a schematic illustration of gyroid-network replication from BCP templates and the fabrication of hybrid solar cells. In this study, the gyroid-forming poly(4-fluorostyrene)-*block*-poly(D,L-lactide) (PFS-*b*-PLA) BCP was spin-cast onto a glass substrate with fluorine-doped tin oxide (FTO) glass by means of bottom-up self-assembly, after which the PLA networks were etched away, leaving the PFS gyroid structures. TiO_2 was deposited on a PFS template by the anodic oxidative hydrolysis of aqueous $TiCl_3$ in a standard three-electrode electrochemical cell. Subsequently, thermal annealing was conducted at 500 °C under an Ar atmosphere for the removal of the polymer

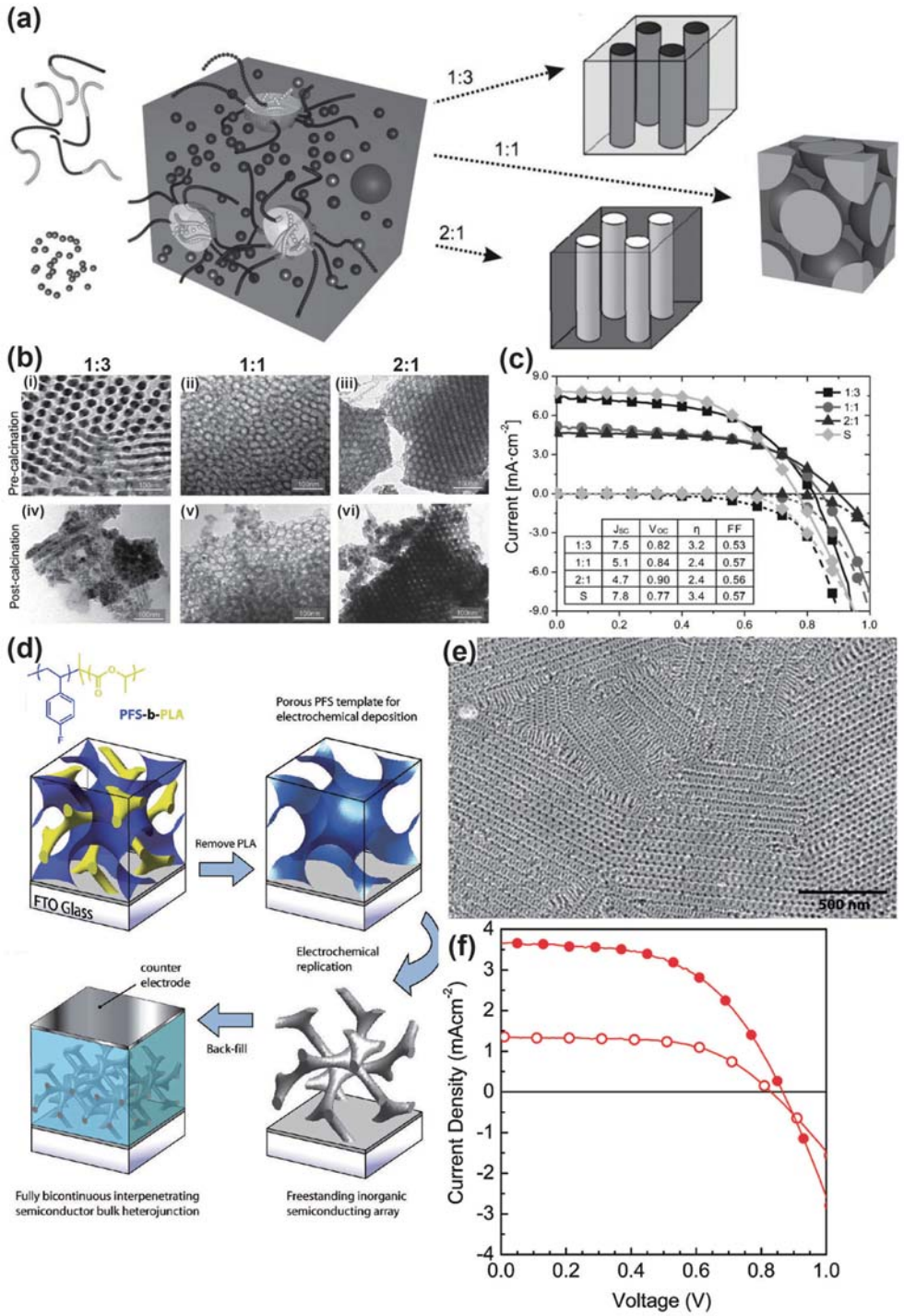

Figure 8. a) Schematic sketch of the self-assembly formation of a TiO_2-BCP composition depending on the morphology. b) Bright-field TEM images of the materials for the different recipes before calcination, i.e., as a hybrid material. The light areas in (i)–(iii) show the organic-rich domains, and the dark areas correspond to the TiO_2-rich domains. iv–vi) TEM images of the calcined material for all three recipes (heated to 500 8C in air). c) Current-density–voltage (J–V) curves of devices made from the three titania recipes (see legends). A reference device fabricated from a standard nanoparticle paste is depicted by the gray diamonds (S in the legend). The inset shows the extracted values for the short-circuit current (J_{sc}), the open-circuit voltage (V_{oc}), the power conversion efficiency (η), and the fill factor (FF) for the four devices shown. d) Schematic representation of the gyroid network replication process from BCP templates and the assembly of hybrid solar cells. e) Surface SEM image of the replicated anatase TiO_2 gyroid network after the oxidative removal of the polymer template. f) The current–voltage characteristics of 400 nm thick solid-state cells sensitized with Z907 (open circles) and D149 (solid circles) with power conversion efficiencies of 0.7% and 1.7%, respectively. The open-circuit voltages are 830 and 870 mV, the short-circuit currents are 1.35 and 3.66 mA cm^{-2}, and the fill factors are 0.60 and 0.54, for the open circles and solid circles, respectively. a–c) Reproduced with permission.[37] Copyright 2010, John Wiley & Sons. d–f) Reproduced with permission.[38] Copyright 2009, American Chemical Society.

template, resulting in a freestanding double-gyroid consisting of TiO_2, as shown in the surface SEM image in Figure 8e. Finally, a bicontinuous bulk-heterojunction solar cell was completed by back-filling the array with a solid-state hole-transporting material and then covering the device with a counter electrode. A solid-state DSSC, including 400 nm anatase TiO_2 gyroid arrays sensitized with D149, showed peak external quantum efficiencies (EQEs) of 33% with an overall efficiency of 1.7%, respectively (Figure 8f). Considering the thickness of the active layer, this result is strongly competitive in comparison with state-of-the-art solid-state DSSCs with similar active-layer thicknesses. This work demonstrated that bicontinuous cubic structures can play a significant role in the performance enhancement of a DSSC.

5. Conclusions

The use of self-assembled BCP technology provides great benefits with regard to device-performance enhancements in the area of next-generation electronic and energy devices. This article discusses recent investigations and developments in the area of non-volatile memory (PCM, RRAM, and flash memory), electrical sensors (gas and biological sensors), and energy devices (TENGs and dye-sensitized solar cells) using the BCP self-assembly process. Interestingly, most electronic and energy devices presented in this progress report, including PCM, RRAM, biosensors, and TENGs (as illustrated in the Sections 2.1, 2.2, 3, and 4.1, respectively) do not need a prepatterned structure for self-assembled nanostructures, which is an inherently complex and high-cost process. These approaches without prepatterned templates may lead to simple and cost-effective process that will benefit industrial implementation.

The approaches based on BCP self-assembly can be divided into three representative areas: i) an adjustment of the surface morphology by self-assembled nanostructures, ii) the insertion of periodic insulating or metallic nanodot arrays onto a target layer, and iii) the supply of nanoscale patterns or templates for the fabrication of nanostructured devices. First, self-assembled BCP thin films can be utilized to obtain diverse surface morphologies, such as dots, lines, holes, and rings. By spatially arranging various self-assembled nanostructures on the desired layer, the surface morphology can be modified for a change of the contact area. Using this approach, the power consumption of a PCM device can be reduced with a decrease in the contact area between the GST phase-change material and a TiN heater electrode. In addition, the output power of a TENG device can be enhanced by adopting a variety of surface morphologies between the top and bottom parts. Secondly, BCP self-assembly technology offers a methodology for forming nanodot periodic arrays placed on target thin-film layers, enabling the nanodot arrays to contribute to the enhancement of the device performance. As a typical example, the reliability of a unipolar RRAM device can be improved by placing self-assembled SiO_x nanodots on a NiO resistive switching material layer for confining the location where CFs are formed. Additionally, the memory window of a charge-trap memory device can be widened by employing binary nanodot arrays consisting of Pt and Au for fabricating multilevel flash memory. Lastly, nanoscale patterns or templates that are formed by the BCP self-assembly process can be applied to fabricate active nanostructured materials such as the charge-storage layer of flash-memory devices, the channel region of field-effect transistors, and the semiconductor regions of dye-sensitized solar cells for performance improvements (as illustrated in Sections 2.3, 3, and 4.2). This patterning approach is most commonly used for dye-sensitized solar cells to enhance their electrode performance levels.[12] In conclusion, the innovative device concepts enabled by BCP self-assembly can provide practical alternatives for improving the performance, efficiency, and reliability of electronic and energy applications.

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