Flexible one diode–one resistor resistive switching memory arrays on plastic substrates†

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Resistive random access memory (RRAM) has been developed as a promising non-volatile memory on plastic substrates for flexible electronic systems owing to its advantages of simple structure and low temperature process. Memory plays an important role in electronic systems for data processing, information storage, and communication, thus flexible memory is an indispensable element to implement flexible electronics. However, cell-to-cell interference existing in a flexible memory array leads to not only undesired power consumption but also a misreading problem, which has been a big hindrance for practical flexible memory application. This paper describes the development of a fully functional flexible one diode–one resistor RRAM device. By integrating high-performance single crystal silicon diodes with plasma-oxidized resistive memory, cell-to-cell interference between adjacent memory cells is effectively prevented, and random access operation of the 1D–1R flexible memory device is successfully achieved on a flexible substrate. The work presented here could provide a useful methodology to realize flexible non-volatile memory with high packing density for flexible electronic applications.

Introduction

Systems on plastic (SoPs) have attracted attention as next generation electronics due to their advantages of outstanding portability, light weight, and convenient interfaces as compared to current electronic devices.1–3 A flexible display for SoP is on the brink of commercialization, as flexible displays were demonstrated with several concept devices in the 2013 International Consumer Electronics Show (CES 2013).4 However, in addition to the display, other parts of electronic devices such as the processor, energy source, and memory should be integrated into a single device on a flexible substrate to perform their respective functions in a SoP.2–4 Among the many components of electronics, flexible memory is the main obstacle for realizing SoP, as it plays a significant role in electronic systems, including data processing, information storage, and communication with external devices.8–10

Resistive random access memory (RRAM) is considered as a promising candidate for flexible memory in SoP due to its advantages of simple structure, high-density integration, low temperature process, high-speed switching property, and low power consumption.10–14 Several research groups have reported flexible resistive memory with a simple crossbar structure based on various materials such as GeO/HfON,10 TiO2,15 SiOx,16 Al2O3,17 Ag2Se,18 and polystyrene/carbon nanotube (PS/CNT).19 Among many materials that have been developed for flexible resistive memory, plasma-oxidized binary metal oxides are of interest owing to their compatibility with a conventional micro-fabrication process.17,20 Moreover, the plasma-oxidation process can provide uniform and reliable resistive switching materials on plastic substrates with high oxidation speed at low temperature. In spite of the strengths of plasma-oxidized metal oxides films, very few attempts have been made to apply them as flexible resistive memory.17

The major issue on flexible resistive memory is cell-to-cell interference occurring through leakage current paths during memory access operation; this is known as a cross-talk problem.15–21 Since the cross-talk problem induces serious failure during memory operation, it limits memory size to just a few bits.25–28 To fabricate a fully functional flexible memory, each memory cell must be integrated with a selection device, and thus they should be formed into one diode–one resistor (1D–1R)9 or one transistor–one resistor (1T–1R) structure,8 which has been a long term obstacle to achievement of SoP because of the absence of high-performance selection devices.8

In terms of integration, as in commercialized phase change memory,7,29 a diode is preferred as a selection component over a transistor because the 1D–1R structure has advantages of
small occupying area, simple design, easy fabrication, and high yield over the 1T–1R structure. However, there are still unresolved issues with flexible diodes on plastic substrates, such as insufficient current density for application as a selection element of memory. To achieve a high density flexible RRAM, the selection diodes should present a high forward current density exceeding \(10^5 \text{ A cm}^{-2}\) and a high rectifying ratio over \(10^6\) for high packing density (>1 Mb), but the previously reported selection diodes built on plastic substrates have not satisfied these specifications.11,12

Herein, we have developed a RRAM with a 1D–1R structure on a plastic substrate. High-performance flexible single crystal silicon diodes13,14 were integrated with copper oxide based resistive memory5 on a plastic substrate to prevent the cross-talk problem. The 1D–1R RRAM unit cells were interconnected with each other through word and bit lines in \(8 \times 8\) arrays to control each memory unit cell independently.6 Finally, the random access memory operation of 1D–1R RRAM on a flexible substrate was successfully performed by utilizing the integrated single crystal silicon diode with an excellent rectifying ratio (\(>10^5\)) and forward current density (\(>10^5 \text{ A cm}^{-2}\)). The obtained results may open up new possibilities of realizing non-volatile memory with high packaging density for high performance flexible electronics.

Experimental

Fabrication process of flexible 1D–1R RRAM

The selection diodes used single crystal doped silicon nanomembranes as active layers. The fabrication began with definition of highly doped regions with boron and phosphorous on a p-type silicon on insulator (SOI) wafer with a 340 nm top Si layer and 1 μm buried oxide (SOITEC). Heavily n and p-doped regions were formed on a p-type Si layer (10 Ω cm) by utilizing a spin-on-dopant (Filmtronic, P509) and boron implantation, respectively, and the SOI wafer was annealed in a rapid thermal annealing system. A photo-lithographically defined layer of SiO2 deposited by plasma enhanced chemical vapor deposition (PECVD) was used as a doping mask. After doping, the underlying buried oxide was removed by a concentrated HF solution in order to release the ultrathin silicon membrane. Doped Si was transferred onto the 50 μm thick polyimide substrate (DuPont, Kapton) with a spin-cast PI precursor (poly(amic acid), Sigma Aldrich) as a thermally curable adhesive. The PI precursor was fully cured at 250 °C for 1 h in a nitrogen atmosphere. The diodes were then isolated by SF6 plasma etching with active region of \(300 \times 300 \mu\text{m}^2\) and cell-to-cell distance of 500 μm. The layers of Au/Cr (200 nm/10 nm) for metal contacts and Cu/Cr (250 nm/10 nm) for bottom electrodes were deposited respectively on anode and cathode regions of diodes using a radio-frequency (RF) sputtering and lift-off process. After the formation of Cu/Cr bottom electrodes, copper oxide was formed by oxygen plasma in an inductively coupled plasma-reactive ion etching (ICP-RIE) system at room temperature. Subsequently, the Al top electrodes with the active area of \(50 \times 50 \mu\text{m}^2\) were formed in the same way as the bottom electrodes (see ES1) for details on the fabrication of a flexible RRAM on a plastic substrate, Fig. S1).

Measurement of the C-AFM sample

For sample preparation, the SET or RESET process of Al/CuO/Cu memory was carried out, and then Al top electrodes were etched by an aluminum etchant. The reading process was performed at a voltage of 0.5 V in contact mode by an AFM equipped with a Pt/Ir-coated Si tip with arm length of 225 μm, width of 28 μm, and thickness of 3 μm.

Device measurement

The electrical characterization of the flexible RRAM device was carried out with a probe station at room temperature using a Keithley 4200-SCS semiconductor characterization system equipped with a pulse measurement unit (Keithley 4225-PMU) and a remote amplifier switch (Keithley 4225-RPM) for ultrafast pulsed I–V measurement.

Results and discussion

Fig. 1a shows a schematic illustration of a flexible 1D–1R RRAM with \(8 \times 8\) arrays on a plastic substrate. A flexible RRAM unit cell consists of a single crystal silicon diode as a selection device, and Al/CuO/Cu layers deposited on the cathode region of the silicon diode for unipolar resistive switching. The selection diode is integrated to prevent cell-to-cell interference during memory operation by utilizing its rectifying property.14 To fabricate single crystal silicon diodes as high performance selection devices of memory, single crystal silicon membranes, which had been doped at high temperature above 950 °C, were arrayed on a plastic substrate.15 The Al/CuO/Cu layers of metal-insulator–metal (MIM) structures were formed at the cathode region of the diode for resistance switching by radio frequency (RF) sputtering and O2 plasma oxidation at room temperature.16 Finally, all memory cells were interconnected with each other through word and bit lines in a passive matrix array for random access operation of the memory.2 The resistive switching mechanism of the CuO based unipolar memory can be explained by the formation and rupture of conductive filaments, as illustrated in the inset of Fig. 1a.17,18 This plasma oxidized copper oxide has the advantage of being compatible with the standard complementary metal–oxide–semiconductor (CMOS) process, and it also provides a low temperature process that is suitable for flexible electronics.17,20

Fig. 1b shows a magnified optical image of the unit cells of the 1D–1R RRAM array. The word (WL) and bit lines (BL) cross each other to control the logic state change of each memory unit cell by forming a passive matrix. The inset of Fig. 1b shows a schematic cross-sectional view of 1D–1R unit cell on a plastic substrate. The anode region of the selection diode and the Al top electrode are connected to the WL and BL, respectively, and spin-cast SU-8 passivation layers provide an interlayer dielectric between the BL and WL. The integrated diodes have a lateral structure in this study, but they can be converted to a vertical structure by adopting epitaxial silicon growth or well-controlled
ion implantation, which can be applied to 1D–1R crossbar structure memory for larger array density.\textsuperscript{24} Fig. 1c displays a photograph of the completed flexible 1D–1R RRAM on a 50 μm thick polyimide film with an active area of 1 × 1 cm\textsuperscript{2}. The inset shows good flexibility of the devices without any mechanical damage when rolled on a glass rod. All fabrication processes on a flexible substrate are carried out at low temperature under 300 °C, which offer stability to devices on plastic substrates.\textsuperscript{37} Along with low fabrication temperature, ultrathin inorganic materials and the simple structure of the device can provide high flexibility as well as high performance on plastic substrates.\textsuperscript{8,38}

Fig. 1d presents a cross-sectional bright-field transmission electron microscopy (BFTEM) image of the MIM structure (185 nm Al/37 nm Cu2O/233 nm Cu) on a plastic substrate. The existence of a copper oxide layer between the top Al and Cu layers can be confirmed through TEM energy dispersive X-ray spectroscopy (EDX) elemental mapping of Al (blue), O (green), and Cu (red) in the upper inset of Fig. 1d. The composition analysis of Cu2O was conducted by X-ray photoelectron spectroscopy (XPS), as shown in the lower inset of Fig. 1d. The main peak (blue line) at 934.78 eV and a shoulder (red line) at 932.93 eV respectively correspond to CuO and Cu2O; these results indicate the coexistence of CuO and Cu2O in the Cu2O layer.\textsuperscript{39,40}

Fig. 2a shows the I–V characteristics of the single crystal diode used as selection device of the memory. The integrated diodes exhibit high-performance electrical properties with a high rectifying ratio of 10\textsuperscript{9} at ±1 V and a current density of 10\textsuperscript{5} A cm\textsuperscript{2} in the forward bias region. The selection devices have sufficient current output to operate unipolar switching memory on plastic substrates where high current over a few mA is needed to cause rupture of conductive filaments.\textsuperscript{41} Furthermore, specifications of this selection diode will be theoretically applied to a high array density memory over 1 Mb.\textsuperscript{25} Fig. 2b shows the typical Cu2O-based unipolar memory switching behavior after a forming process (see Fig. S3 in ESI†) for the forming process of resistive memory). The resistance state of RRAM switched to the HRS at 0.6 V, as the voltage is swept from zero to a positive voltage: the RESET process. By sweeping the applied voltage on the top electrode with current compliance of 1 mA, the device is returned from the HRS to the LRS at 2.3 V: the SET process. The upper inset in Fig. 2b shows linear I–V characteristics of Al/Cu2O/Cu resistive memory in positive and negative voltage regions, indicating that our resistive change material shows unipolar resistive switching where the resistance state switching is independent of the voltage polarity.\textsuperscript{13} It is interesting that the resistances of the HRS and LRS decreases with increased temperature, as presented in the lower inset of Fig. 2b. This resistance behavior implies that the conduction mechanism in the LRS is dominated by ionic filaments that are typically composed of oxygen vacancies, not metallic filaments.\textsuperscript{39,40}

In order to characterize the 1D–1R unit cell in 8 × 8 arrays, electrical properties were evaluated in dc sweep and pulse modes. Fig. 3a shows the I–V characteristics of the flexible 1D–1R memory unit cell in the dc sweep mode with its circuit diagram. While the diode prevents resistance switching of the Al/Cu2O/Cu layers due to its rectifying property in the reverse bias, resistance switching of the 1D–1R device is successfully
observed in forward bias with a SET voltage of 2.5 V, a RESET voltage of 1.8 V, and a resistance ratio of $10^2$ between the LRS and HRS at 1 V (reading voltage). Fig. 3b shows the electrical response of 1D–1R memory to the input voltage pulses: 5 ms/5 V pulse for the SET, and 5 ms/2 V pulse for the RESET, and 10 ms/1 V for the reading. This pulse mode of memory operation is more practically significant than the dc sweep mode, because actual memory devices have been driven by voltage pulses. In the beginning, the resistance state of 1D–1R memory is set to the HRS. As pulse voltage of 5 V is applied for the SET process, the resistance value of the memory is turned to a LRS of 1.23 kΩ, and this resistance state of the device reverts to a HRS of 4.31 MΩ by applying a voltage pulse of 2 V. The resistance switching phenomenon of 1D–1R memory occurs stably and consistently in repeated pulse mode, as shown in Fig. 3b. The detailed transition response waveforms for the SET and RESET processes are presented in the left (current) and right (voltage) insets of Fig. 3b, respectively. In the case of the SET process, the electric current value abruptly increases after 15 μs has passed since the voltage of the pulse reached 5 V and the response current is maintained at 1.12 mA due to current compliance. On the other hand, 550 μs with a pulse height of 2 V is required to convert the resistance state of the unit cell to the HRS (see ESI† for electrical response of memory cell to much shorter voltage pulse, Fig. S6).

To investigate the reliability of the flexible 1D–1R RRAM, endurance and retention tests were performed. Fig. 3c shows the results of the endurance test conducted by applying repeated voltage pulses, depicted in the inset, on the memory cell of 1D–1R RRAM. During more than 100 repeated switching cycles, the two states retain their resistance values without significant variation, although there is slight fluctuation during repeated cycles. The retention characteristics of the 1D–1R device were also assessed at a read voltage of 1 V to evaluate the data storage ability in the HRS and LRS. As shown in Fig. 3d, the 1D–1R memory has a stable retention property of up to $10^5$ s at room temperature. These results show that the 1D–1R devices have remarkable reliability performance on flexible substrates.

Bending tests as a function of bending radius and bending cycles were conducted to confirm the mechanical reliability of the 1D–1R memory on a plastic substrate for flexible electronic application. The 1D–1R memory shows almost the same resistive switching property under different bending radii from 50 to 10 mm, which corresponds to various surface strains from 0.05 to 0.25%, as shown in Fig. 4a. Similarly, Fig. 4b presents that 1D–1R RRAM retains its resistance ratio between HRS and LRS without significant degradation during repeated bending cycles, which demonstrates that the 1D–1R RRAM also has excellent mechanical robustness.

Color maps according to the resistance distribution of 64 memory cells in a 8 × 8 array were prepared to examine the uniformity of memory cells and are presented in Fig. 4c and d for the HRS and the LRS, respectively. Although some cells
denoted by black color do not work due to defects generated during the transfer process, the final yield of the integrated device reaches 85–90%, and the device yield can be improved further by adopting an automated fabrication process. Interestingly, the distribution of the LRS is very narrow, but the resistance value of the HRS ranged from $10^5$ to $10^{10}$ Ohm. This may arise from the variation of the gap distance between the electrodes and conductive filaments in the Cu$_2$O layer, induced by nonuniform rupture of the conductive filament during the RESET process. However, the resistance value between the lowest value of the HRS cells and the highest value of the LRS cells demonstrates good separation with a ratio of more than $10^2$, as shown in Fig. 4e (see ESI† for details of statistical analyses of 1D–1R unit cells).

We conducted random access operation of $3 \times 3$ flexible 1D–1R RRAM cells, as schematically illustrated in Fig. 5a, and their operation conditions are presented in Fig. 5b. The initial state of all cells is set to the HRS. By applying the SET pulse on the word lines, the $(1, 1), (1, 2), (1, 3), (2, 3), (3, 3), (3, 2), (3, 1)$, and $(2, 1)$ cells are sequentially changed from the HRS to the LRS (the writing process, see Fig. S12 in ESI†). The READ pulse is then applied to the $(2, 2)$ cell in order to read the resistance state of the $(2, 2)$ cell. The measured resistance value of the selected cell $(2, 2)$ in the $3 \times 3$ 1D–1R array corresponds to the HRS (751 kOhm), indicating that the integrated diodes effectively suppress unintended current paths. If there is no selection device, the correct reading process is impossible due to the sneak current paths, as represented by the red dotted lines in Fig. 5c (see ESI† for the reading operation of 1R memory array without selection devices). On the contrary, an accurate reading process is possible in the 1D–1R RRAM, because the selection device does not permit current paths through neighboring low resistance states.
(see Fig. 5d). Finally, we conducted the SET process of the (2, 2) cell by applying a SET pulse, and all memory cells were changed back to the HRS by applying the RESET pulse to demonstrate the erasing processa (see ESI† for details of the writing/reading/erasing process).

Conclusions

In summary, we demonstrated a flexible 1D–1R RRAM with 8 × 8 arrays composed of high-performance silicon diodes and a resistive change material. The stability and reliability of flexible RRAM were confirmed from an endurance/retention test and a statistical analysis. The developed devices also showed excellent mechanical reliability in terms of bending radii and times tests. Finally, the proposed flexible 1D–1R RRAM demonstrated random access operation including write/read/erasing on a plastic substrate due to the rectifying property of integrated diodes. This flexible 1D–1R RRAM technology shows the possibility of realizing high packing density memory on plastic substrates, and may offer an important breakthrough for realizing a flexible electronic system through integration with flexible large-scale integration (LSI). We are currently developing this technology by adopting wafer-level transfer protocol on plastic substrates to achieve high density memory and cost reduction.a

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Notes and references

Supplementary Information to “Flexible One Diode-One Resistor Resistive Switching Memory Arrays on Plastic Substrates”

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1. Device fabrication process

Fig. S1 shows schematics of the fabrication steps for flexible 1D-1R RRAM on a plastic substrate. Patterned silicon nanomembranes were transferred from a silicon on insulator (SOI) wafer onto a polyimide substrate (DuPont, Kapton) with a spin-cast PI precursor (Poly(amic aci(d), Sigma Aldrich) as an adhesive.\textsuperscript{1,2} After transfer process, active regions (300 × 150 μm²) of diodes were isolated by photolithography and SF₆ plasma etching. The PI precursor was fully cured at 250 °C for 1h in a nitrogen atmosphere [Fig. S1a]. The layers of Au/Cr (200 nm/10 nm) for metal contacts and Cu/Cr (250 nm/10 nm) for bottom electrodes were deposited respectively on anode and cathode regions of diodes using a radio-frequency (RF) sputtering and lift-off process [Fig. S1b]. Copper oxide layers were formed by plasma oxidation process in an inductively coupled plasma-reactive ion etching (ICP-RIE) system with RF power of 200 W for 10 min at room temperature [Fig. S1c]. After formation of the copper oxide layer, the Al top electrodes were formed in the same way as the bottom electrodes [Fig. S1d]. The bit lines and word lines of Au/Cr (200 nm/10 nm) were patterned sequentially through a radio-frequency (RF) sputtering and wet etching. Spin-cast SU-8 layer with photo-lithographically opened interconnect access holes were employed as the interlayer dielectric between the metal layers. [Fig. S1e and S1f].
Fig. S1. Detail schematic illustration of the process for fabricating 1D-1R RRAM on a plastic substrate. (a) Transfer-printing of silicon nanomembrane onto a polyimide substrate. (b) Deposition of metal layers (c) Plasma oxidation for forming copper oxide layer. (d) Deposition of Al top electrodes. (e-f) Interconnection of memory cells through word and bit lines.
Fig. S2. A magnified optical image of the flexible 1D-1R device. The inset shows 1D-1R unit cell in memory array. The active area of the diode and resistive memory are $300 \times 150 \ \mu m^2$ and $50 \times 50 \ \mu m^2$, respectively.
2. The forming process of flexible RRAM.

Fig. S3a-b shows the I-V properties of a forming, RESET, and SET processes of 1R and 1D-1R memory. As shown in Fig. S3a-b, the forming processes are observed at 3.6 V for 1R and 3.8 V for 1D-1R, respectively. After the forming process, the developed device shows reproducible resistive switching characteristics.

**Fig. S3.** (a) The I-V curves of the 1R RRAM. The forming voltage is 3.6 V. (b) The I-V curves of the 1D-1R RRAM. The forming voltage is 3.8 V.
3. The DC I-V curves of flexible 1D-1R memory & Statistical analysis of flexible silicon diode

Fig. S4a shows the cumulative probability data of both the forward and reverse state resistance at ±1 V measured by I-V curves of 40 silicon diodes. The inset of Fig. S4a shows the rectifying ratio distribution depicted by a box-whisker plot obtained from the I-V curves of 40 silicon diodes. Fig. S4b shows the switching I-V curves of the 1D-1R memory cell. During the SET operation in dc voltage sweep mode, a compliance current of 1 mA was selected to avoid the permanent breakdown of 1D-1R device. This result presents that the flexible 1D-1R memory exhibits stable resistive switching cycles. The inset of Fig. S4b shows the SET and RESET voltage distribution of the flexible 1D-1R memory cell depicted by a box-whisker plot obtained from the I-V curves of 50 switching cycles.

Fig. S4. (a) The statistical characteristics of silicon diodes. The inset shows the rectifying ratio distribution of silicon diodes (b) The DC I-V curves of the flexible 1D-1R RRAM in forward bias region. The inset presents the SET and RESET voltage distributions of flexible 1D-1R memory cell.
4. Statistical analysis of flexible 1D-1R memory

Fig. S5a shows the cumulative probability data of both the LRS and HRS measured by I-V curves of 55 memory cells. The LRS exhibits narrow distribution, but distribution of the HRS shows broad distribution, which may be related to the variation of the ruptured filament path length. Fig. S5b shows the current density-voltage characteristics of the silicon diode in the forward bias. The silicon diode provides the sufficient current density (>10⁵ A/cm²) to operate unipolar resistive memory. The inset of Fig. S5b shows the forward state resistance of the silicon diode according to the applied voltages. This result shows non-linear behavior of resistance state in forward bias, and this non-linearity plays a significant role as a buffer resistor enhancing programming margin of the 1D-1R device. Fig. S5c shows the SET and RESET voltage distribution of the flexible 1D-1R RRAM depicted by a box-whisker plot obtained from I-V curves of 55 memory cells. When compared with voltage distribution of 1R memory cell without selection diodes in the inset of Fig. S5c, it is found that the programming voltage margin between the SET and RESET is greatly stabilized by integrating selection diodes. This result shows that the silicon diode plays important roles of a selection device to prevent cell-to-cell interference as well as a buffer resistor to suppress excessive current flow during SET process. Fig. S5d shows the retention characteristics of flexible 1D-1R device measured at 80 °C, demonstrating that no significant change of the resistance occurs in both the LRS and HRS for 10⁴ s.
Fig. S5. (a) Cumulative probability data of each the HRS and LRS obtained from I-V curves of 55 unit cells. (b) Current density-voltage characteristics of a silicon diode under the forward bias. The inset presents the forward state resistance of the silicon diode according to the applied voltages. (c) SET and RESET voltage distributions of the 1D-1R RRAM depicted by a box-whisker plot obtained from I-V curves of 55 unit cells. The inset presents the SET and RESET voltage distributions of 1R memory cells without selection diodes. (d) Retention characteristics of flexible 1D-1R RRAM measured at 80 °C.
5. Electrical pulse measurement of flexible 1D-1R memory

The electric pulse measurement of 1D-1R memory was conducted to examine the SET and RESET voltage pulse height and width. 10 switching cycles can be achieved with 500 ns/5 V (SET pulse) and 500 μs/2 V (RESET pulse), as shown in Fig. S6. The insets of Fig. S6 present the transition response current waveforms for the SET (left) and RESET processes (right). These results show that the SET and RESET processes are successfully observed at 500 ns and 500 μs of pulse width, respectively.

**Fig. S6.** Resistive switching characteristics measured by repeated voltage pulses. The insets show electrical response current waveforms for the SET (left) and RESET (right) processes.
6. Resistive switching characteristics under the bended condition

Fig. S7a-b shows the resistive switching characteristics obtained from I-V curves of 10 unit cells as a function of different bending radii and times. As shown in Fig. S7a-b, the 1D-1R device exhibits almost same resistive switching behavior under various bending radii and bending times, which demonstrates that the developed flexible memory has good mechanical stability under the bended condition.

**Fig. S7.** The statistical characteristics of mechanical reliability obtained from I-V curves of 10 unit cells. (a) The resistance values as a function of different radii. (b) The bending fatigue test results.
7. Conduction mechanisms of the memory in the LRS and HRS

To further understand the conduction mechanisms of the Al/Cu$_x$O/Cu resistive memory, Fig. S8 shows the double logarithmic plot of I-V characteristics of the Al/Cu$_x$O/Cu resistive memory. The log I-V plot of the LRS clearly shows an Ohmic conduction behavior with a slope of 1, which is originated from the formation of conductive filaments in the copper oxide layer. The log I-V plot of HRS can be divided into three region; Ohmic conduction behavior region ($I \propto V$), square dependence region ($I \propto V^2$), and steep current increasing region ($I \propto V^{8.6}$). This behavior can be explained by trap-controlled space-charge-limited conduction (SCL(C) mechanism that happens in the filament-free region, which is generally indicated by an increasing slope value from Ohm’s law ($I \propto V$) to Child’s law ($I \propto V^2$), as voltage increases.$^6,7$

Fig. S8. A double-logarithmic plot of the I-V characteristics during the SET and RESET process.
8. The reading operation for 2 × 2 1R memory cells

The fabricated Cu$_x$O RRAM device with 2 × 2 cross-bar structure is shown in Fig. S9. Fig. S10 illustrates the writing process of the 1R memory cells with 2 × 2 array. Before the writing process, the initial state of all memory cells is set to the HRS. Fig. S10a shows that resistance state of the selected (1,1) cell is converted from the HRS to the LRS while other memory cells maintain their original HRS states. Initially, the high resistance state of 869 kΩ of (1,1) cell is read with the reading voltage of 0.1 V. To change the resistance state of (1,1) cell from HRS to LRS, the dc voltage is applied to the selected word and bit lines. After switching the resistance state, the low resistance state of 89 Ω of (1,1) cell is read with the same reading voltage. Similarly, the resistance states of other memory cells are sequentially converted from HRS to LRS in the order of (1,2), (2,1) through the writing process described in the above. After (1,1), (1,2), and (2,1) cells are set to the LRS, the reading voltage is then applied to the (2,2) cell in order to read the resistance value of the (2,2) cell, and the resistance value of (2,2) cell is 148 Ω. From this result, we experimentally measured the cell-to-cell interference occurring through leakage current paths in 1R memory cells without the selection diodes.

![Fig. S9. A 2 × 2 cross-bar array Cu$_x$O RRAM device.](image)
**Fig. S10.** The writing process of $2 \times 2$ 1R memory cells. Red color denotes the HRS (logic state “0”) and blue color denotes the LRS (logic state “1”).
9. The random access operation for 3 × 3 flexible RRAM cells

Fig. S11 shows a schematic of 3 × 3 1D-1R RRAM cells (Fig. S11a and its corresponding circuit diagram (Fig. S11b). The initial state of all memory cells was set to the HRS, represented in red (logic state “0”).

![Fig. S11. (a) Schematic of 3 × 3 1D-1R RRAM cells. (b) Circuit diagram corresponding to Fig. S11a. Red color denotes the HRS (logic state “0”).](image)

A. Writing process

Fig. S12 illustrates the writing process of the flexible 1D-1R RRAM cells with 3 × 3 array. Fig. S12a shows that resistance state of the selected (1,1) cell is converted from the HRS to the LRS while other memory cells maintain its original HRS state. Initially, the high resistance state of 220 kΩ of (1,1) cell is read with the reading voltage pulse of 5 ms/1 V on a selected word line (WL1). To change the resistance state of (1,1) cell from HRS to LRS, the voltage pulse of 5 ms/5 V (SET pulse) is applied on selected word line (WL1). After switching resistance state, the low resistance state of 0.53 kΩ of (1,1) cell is read with same reading voltage pulse. Similarly, resistance states of other memory cells are sequentially converted from HRS to LRS in the order of (1,2), (1,3), (2,3), (3,3), (3,2), (3,1), (2,1), (2,2) through the writing process described in the above.
Fig. S12. The writing process of $3 \times 3$ flexible 1D-1R RRAM cells. Red color denotes the HRS (logic state “0”) and blue color denotes the LRS (logic state “1”).
B. Erasing process

Fig. S13 illustrates the erasing process of the flexible 1D-1R RRAM cells with 3 × 3 array. Fig. S13a shows that resistance state of the selected (2,2) cell is converted from the LRS to the HRS while other memory cells maintain its original LRS state. Initially, the low resistance state of 0.44 kΩ of (2,2) cell is read with the reading voltage pulse of 5 ms/1 V on a selected word line (WL2). To change the resistance state of (2,2) cell from LRS to HRS, the voltage pulse of 5 ms/2 V (RESET pulse) is applied on selected word line (WL2). After switching resistance state, the high resistance state of 780 kΩ of (2,2) cell is read with same reading voltage pulse. Similarly, resistance states of other memory cells are sequentially converted from LRS to HRS in the order of (2,1), (3,1), (3,2), (3,3), (2,3), (1,3), (1,2), (1,1) through the erasing process described in the above.

Fig. S13. The erasing process of 3 × 3 flexible 1D-1R RRAM cells. Red color denotes the HRS (logic state “0”) and blue color denotes the LRS (logic state “1”).
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