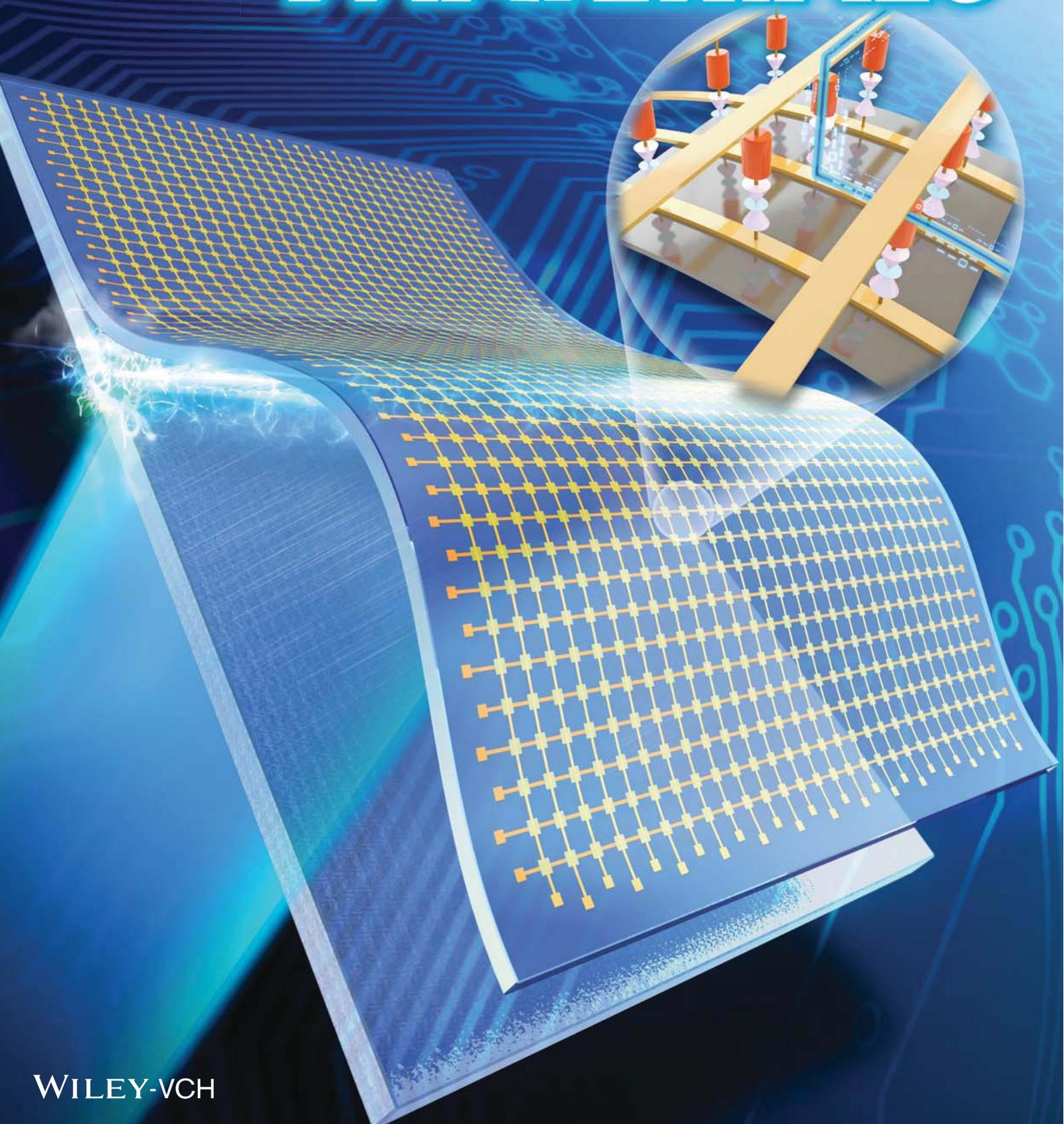


Vol. 26 • No. 44 • November 26 • 2014

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ADVANCED MATERIALS



WILEY-VCH

Flexible Crossbar-Structured Resistive Memory Arrays on Plastic Substrates via Inorganic-Based Laser Lift-Off

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Flexible electronics have been extensively investigated in hopes of realizing system-on-plastic (SoP) applications as the next-generation technology in various areas, ranging from consumer electronics to bio-integrated medical devices.^[1–3] Flexible memory in particular is regarded as an integral component for SoP applications because of its crucial role in data processing, storage, and communications with external devices.^[4–7] A number of research groups have explored a variety of organic-based flexible memories including flash memory,^[8,9] ferroelectric memory,^[10] and resistive memory,^[4,11] directly fabricated at relatively low temperature on flexible substrates using spin-coating, roll-to-roll, and other processes. Although these organic-based flexible memories have been well-established with the capability of achieving flexible electronics over large areas in a cost-effective manner, there are still big challenges in developing high-density flexible memory with high performance, including how to resolve insufficient performance arising from inherent material properties and the non-compatibility with complementary metal–oxide–semiconductor (CMOS) processes.^[12–14]

To address these limitations, there have been attempts to transfer printed inorganic materials onto flexible substrates as a method of incorporating the outstanding performance of inorganic materials processed at high temperature on rigid substrates.^[15] Several conceptual high-performance devices, such as integrated circuits,^[16] inorganic light-emitting diodes,^[17,18] and nanogenerators,^[19,20] have been successfully fabricated by transferring micropatterned inorganic nanomembranes onto flexible substrates. This transfer printing method has enabled excellent electrical performance, exceeding those previously demonstrated on plastic substrates.

Resistive random access memory (RRAM) has been considered a promising non-volatile memory due to its simple structure, high switching speed, low power consumption, and high packaging density.^[21–23] In our previous studies, we have demonstrated two types of flexible RRAMs (i.e., a one transistor–one memristor (1T–1M)^[5] and one diode–one resistor (1D–1R)^[7] structure). These structures were made from ultrathin single-crystalline silicon membranes that were printed onto plastic

substrates to prevent cell-to-cell interference.^[24] However, the difficulties of multilayer metal interconnection caused by the inevitable alignment inaccuracies during the transfer process aggravated attempts to scale down to nanometer regime.^[25] In particular, putting aside the expense of silicon-on-insulator (SOI) wafers,^[14] the fundamental thermal instabilities of polymers^[26] block their integration with other functional electronic materials/devices because a high-temperature process is required after transfer printing, which is incompatible with polymer materials, and this has consistently restrained the achievement of high-density flexible memory for SoP technology.^[14,25]

In recent years, there have been novel approaches for transferring entire devices that have been fully fabricated on rigid substrates at high temperature to flexible substrates. Several clever methodologies such as chemical/mechanical thinning of the wafer,^[25,27] epitaxial layer transfer,^[28] and stress-controlled exfoliation^[13,29,30] have been explored to achieve mechanical flexibility, high performance, nanoscale features, nanoscale alignment, and multi-functionality. Although these works have shed a positive light on high-performance flexible electronics, including static random access memory (SRAM) on flexible substrates,^[13] major issues such as the sophisticated process, limited applicability, high cost, and unpredictability of the transfer still remain to be resolved.^[13,14]

Herein, we report a conceptual strategy for the fabrication of flexible memory employing a one selector–one resistor (1S–1R) crossbar structure^[22] on a plastic substrate via an inorganic-based laser lift-off (ILLO) process. The 32×32 1S–1R crossbar memory arrays for 1 kbit of flexible memory were fabricated with an inorganic laser-reactive exfoliation layer on a rigid glass substrate using a conventional CMOS process, and then subsequently transferred to a flexible substrate through the ILLO process. Structural design was optimized by finite element analysis (FAE) simulations to predict and prevent possible thermal damage during laser irradiation. Based on the simulations, the dry ILLO process was applied for the large-area transfer of the memory device onto a flexible substrate without mechanical damage during the transfer process. Finally, the 1S–1R RRAM cells, formed on a plastic substrate, were successfully evaluated in a worst case scenario^[31] influenced by the suppression of a sneak path of integrated selectors. We strongly believe that the proposed approach using ILLO could be applied to diverse high-performance electronics, such as the driving circuits for displays, and even to electronic devices that require extremely-high-temperature processes, such as doping and crystallization, by adapting exfoliation layers and substrates.

Figure 1a schematically illustrates the fabrication steps of the flexible 1S–1R RRAM on a plastic substrate enabled by the

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DOI: 10.1002/adma.201402472

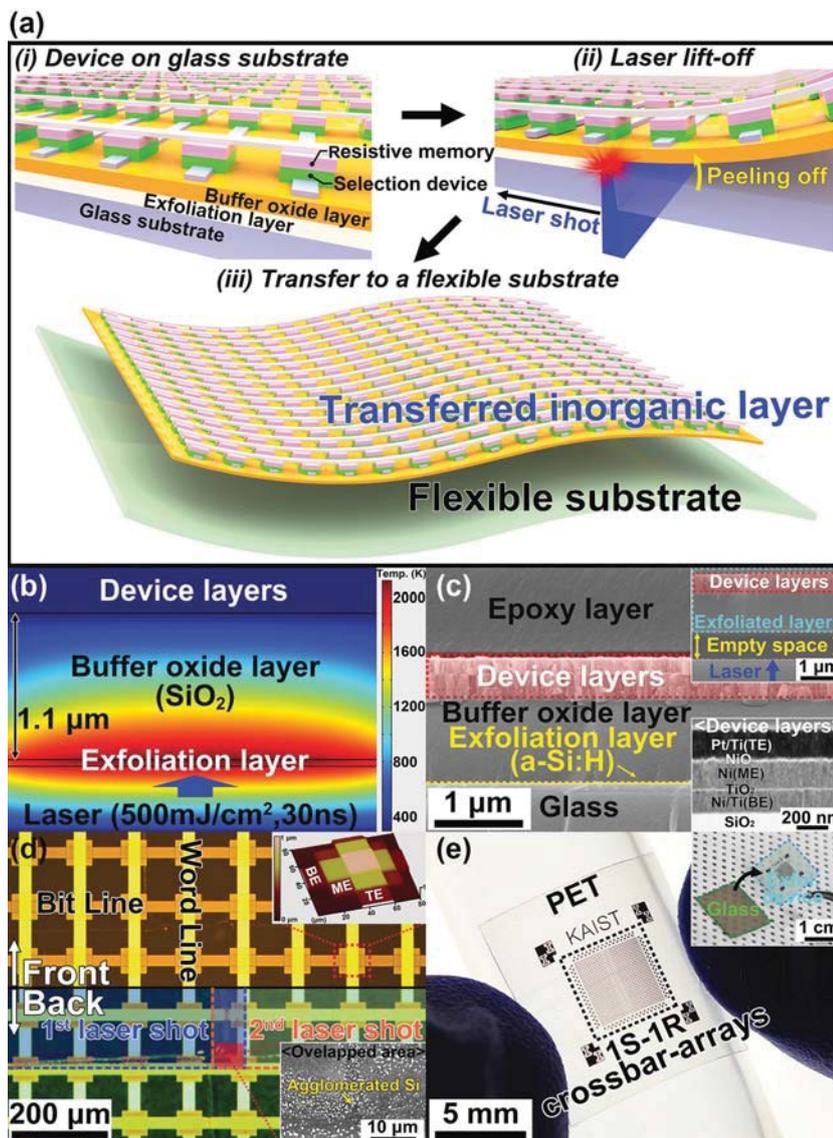


Figure 1. a) Schematic illustrations of the process for fabricating flexible crossbar-structured memory on a plastic substrate via the ILLO method. b) FEA simulation of temperature distribution when the energy density of $500 \text{ mJ}/\text{cm}^2$ is injected into the exfoliation layer. c) A cross-sectional SEM image of the overall structure and each layer on a glass substrate before the ILLO process. The upper inset shows a cross-sectional image of a sample after being laser-irradiated from the back of the glass substrate. The lower inset is a cross-sectional BFTEM image of device layers between the epoxy passivation layer and buffer oxide layer. d) A magnified optical image of the front side (upper region) and back (lower region) of the memory array transferred onto a flexible substrate. The upper inset shows an AFM image of a unit cell in the memory array. The lower inset presents an SEM image of the flipped side after the ILLO process to elucidate the striped patterns on the back of the memory array. e) A photograph of the flexible RRAM device on a plastic substrate. The inset shows its detachment process from a glass substrate after laser irradiation.

ILLO process. A unit cell of RRAM on a glass substrate consists of a selection device for preventing cell-to-cell interference and resistive memory for resistive switching. In this study, a selector is used as the selection device for the high-density crossbar memory, utilizing bipolar resistive switching materials.^[22,32] All memory cells are interconnected through bottom and top electrodes, which are electrically isolated by insulators,

forming a crossbar structure. It is important to note that an exfoliation layer and a buffer oxide layer are deposited between the glass substrate and the RRAM device layer (Figure 1a(i)).

A XeCl excimer laser with a wavelength of 308 nm, which is well-established in the display industry for low-temperature polysilicon (LTPS), was irradiated through the back side of the glass substrate to reduce the adhesion between the exfoliation layer and the substrate, thus finally detaching just the upper inorganic layer from the substrate, as shown in Figure 1a(ii). This ILLO process is explained by localized melting,^[33] vaporizing,^[34] or dissociating of the laser-reactive exfoliation layer^[35] as a result of the laser-materials interaction. In previous studies, we had demonstrated the easy transfer of a large-area lead zirconate titanate (PZT) thin film^[33] and gallium nitride (GaN) thin film^[36] onto flexible substrates via a laser lift-off (LLO) process, demonstrating that PZT, GaN, and other inorganic materials can be employed as the exfoliation layer for flexible electronics. In other words, by selecting an inorganic exfoliation layer and substrate that are suitable for the process temperature, further process stability can be guaranteed even at temperatures as high as $1000 \text{ }^\circ\text{C}$ or above.^[34]

A buffer oxide layer supports the upper device layer by compensating internal stress during the ILLO process, playing a key role as a thermal buffer layer, which blocks heat flow generated during the laser-induced exfoliation.^[37] In addition to controlling the duration time of the laser shot, the thickness of the buffer oxide layer would be an important factor for minimizing thermal damage to the device layers in the ILLO process. Finally, the exfoliated layers are transferred onto a receiver plastic substrate coated with UV-sensitive polyurethane (PU, Norland optical adhesive, No. 73) as an adhesive (corresponding to Figure 1a(iii)); more details can be found in the Supporting Information (SI) regarding the fabrication of a flexible RRAM on a plastic substrate (Figure S1).

Finite element analysis (FEA) simulations using COMSOL software were conducted to determine the optimal structure to guarantee

that the buffered oxide layer would be effective as a thermal barrier to prevent damage from the laser-irradiation-induced heat flow. The analysis was made based on the calculations determining the temperature distribution between the exfoliation layer and the buffered oxide layers during the ILLO process. Figure 1b shows the simulated temperature distribution between the exfoliation and the buffered oxide layers during

the ILLO process. Through this simulation, we could confirm that heat flow generated on the exfoliation layer by laser irradiation with a high energy density of 500 mJ/cm^2 and duration time of 30 ns could be blocked by a buffer oxide layer of $1.1 \mu\text{m}$ thickness.^[37]

Figure 1c shows cross-sectional scanning electron microscopy (SEM) images of the overall structure of each layer on a glass substrate prior to the ILLO process. In this study, 50-nm-thick hydrogenated amorphous silicon (a-Si:H) deposited by plasma-enhanced chemical vapor deposition (PECVD) at $300 \text{ }^\circ\text{C}$ was selected as the exfoliation layer. The XeCl laser light can pass through the alkali-free glass substrate (Nippon Electric Glass, OA-10G, thickness of $500 \mu\text{m}$) with over 70% of transmittance at the wavelength of 308 nm ,^[38] and the light can eventually reach the a-Si:H film. The laser causes the a-Si:H film to melt and release hydrogen, thus weakening the adhesion between the a-Si:H film and the glass substrate.^[39] The resulting poor adhesion enables entire device layers to be easily and safely separated from the glass substrate without any significant mechanical deformations on the device and buffer oxide layers. Based on the simulation in Figure 1b, silicon oxide with a thickness of $1.1 \mu\text{m}$ was deposited by PECVD between the device and the exfoliation layers. Including the exfoliation and the buffer oxide layers, all materials used in the present study were inorganic-based, enabling high-temperature processing, in contrast with organic-based material processes.

The mechanical stability of the ILLO process was proven by cross-sectional SEM images after laser irradiation. As shown in the upper inset of Figure 1c (and SI: Figure S3a), neither cracks nor wrinkles are observed over the entire area of the sample after the optimized ILLO process. It is well-known that mechanical instabilities such as cracks and wrinkles can be created by competition between in-plane and out-of-plane stresses.^[40] In the present study, stress relaxation and stability of the ILLO process were achieved by optimizing laser duration and controlling the thickness of the buffer oxide layer from the view points of thermal and mechanical stabilities (see the SI for details on the characterization of the mechanical properties as the thickness of the buffer layer is varied, Figure S2).

The lower inset of Figure 1c shows a detailed cross-sectional bright-field transmission electron microscopy (BFTEM) image of the device layers. Ti/Ni bottom electrodes (BEs) and a Ni middle electrode (ME) were patterned by radio-frequency (RF) sputtering and lithographic lift-off on the glass substrate. The 10-nm-thick TiO_2 film was deposited by atomic layer deposition (ALD) between the BEs and ME to form a Schottky contact.^[41] For resistance switching, NiO_x and Pt top electrodes (TEs) were formed by O_2 plasma oxidation^[7,42] and RF sputtering at room temperature, respectively. The resistive switching mechanism of the Ni/ NiO_x /Ti/Pt resistive switching layers could be explained by the formation and rupture of conductive filaments due to the migration and diffusion of oxygen ions.^[7,43]

A magnified optical image of the front (upper region) and back (lower region) of the 32×32 RRAM array after transfer onto a flexible substrate is presented in Figure 1d. The word-lines (WL) and bit-lines (BL) corresponding to the Pt TEs and Ni BEs form the crossbar structures, assuring control over the logic state change of each memory unit cell. The upper inset in Figure 1d shows an atomic force microscopy (AFM) height

image of the fabricated RRAM unit cell with a line width of $25 \mu\text{m}$. The ME has a square shape with a tolerance of $\pm 15 \mu\text{m}$ between the TEs and BEs ($55 \mu\text{m} \times 55 \mu\text{m}$) for electrical isolation of the memory cell from the neighboring cells.^[44]

We examined the striped patterns on the back side of the transferred layer, which correspond to the overlapped areas created by the first and second 2D ($620 \mu\text{m} \times 620 \mu\text{m}$) laser shots. To clarify these patterns, SEM observation and X-ray photoelectron spectroscopy (XPS) analysis were carried out on the lower side of the exfoliated layers after the ILLO process. The SEM image in the lower inset of Figure 1d confirms that agglomerated particles are randomly distributed on the thin side of the buffer oxide layer. Through XPS analysis, it can be confirmed that these agglomerations originated from the silicon and could be removed by SF_6 plasma (SI: Figure S4(inset)).

Figure 1e displays a photograph of the fabricated flexible 1S–1R RRAM on a $50\text{-}\mu\text{m}$ -thick flexible polyethylene terephthalate (PET) film with an active area of $0.5 \text{ cm} \times 0.5 \text{ cm}$. This flexible memory retains considerable bendability, as shown in Figure 1e, due to the ultrathin inorganic materials and the optimized device structure. The inset in Figure 1e shows that a glass substrate is being detached from the exfoliated device after the ILLO process; this method can be easily applied to a wafer-scale substrate (SI: Figure S3b), thus overcoming the size-related restrictions that have been challenging in the field of flexible electronics. After device layers are exfoliated, the remaining sacrificial substrates could be reused multiple times, which would be beneficial in terms of cost-effectiveness.

Figure 2a depicts the schematic structure of the vertically stacked 1S–1R RRAM unit cell and employed materials with the corresponding circuit diagram. The selector is composed of a Ni BE, TiO_2 , and a square-shaped Ni ME. The inserted TiO_2 layer forms a Schottky barrier between the Ni BE and ME, enabling the memory cell to have non-linear current–voltage (I – V) characteristics to suppress sneak current.^[32,41] The NiO_x film is monolithically formed on the ME by O_2 plasma, between the ME and Pt TE, for the resistive switching.^[7] The symmetric and non-linear I – V characteristics of the Ni/ TiO_2 /Ni selector are presented in Figure 2b on a semi-logarithmic scale, and in the left inset on a linear scale. It can be confirmed that the non-linear current characteristics come from Schottky emission over the Ni/ TiO_2 barrier by linear fitting of $\log(I)$ versus $V^{1/2}$ for the positive voltage region,^[45] as shown in the right inset of Figure 2b.

The I – V characteristics of the flexible 1S–1R memory unit cell in the DC sweep mode are presented in Figure 2c, with its circuit diagram. Fundamentally, Ni/ NiO_x /Pt shows unipolar resistive switching (URS) where the resistance state switching is "independent" of the voltage polarity,^[21] which means that it can work like bipolar switching. The device is switched from the high-resistance state (HRS) to the low-resistance state (LRS) at the negative SET voltage (V_{SET}) of -4.2 V and returned to the HRS at the positive RESET voltage (V_{RESET}) of 3 V . By integrating the resistive switching element into the selector, current increases exponentially by 500 times from half of the reading voltage ($1/2V_{\text{read}} = 1 \text{ V}$) to the reading voltage ($V_{\text{read}} = 2 \text{ V}$) [the nonlinearity factor $\alpha = I(V_{\text{read}})/I(1/2V_{\text{read}}) > 500$], in contrast to the linear I – V characteristics of the 1R device in the inset of Figure 2c. This result indicates that a sneak current can be

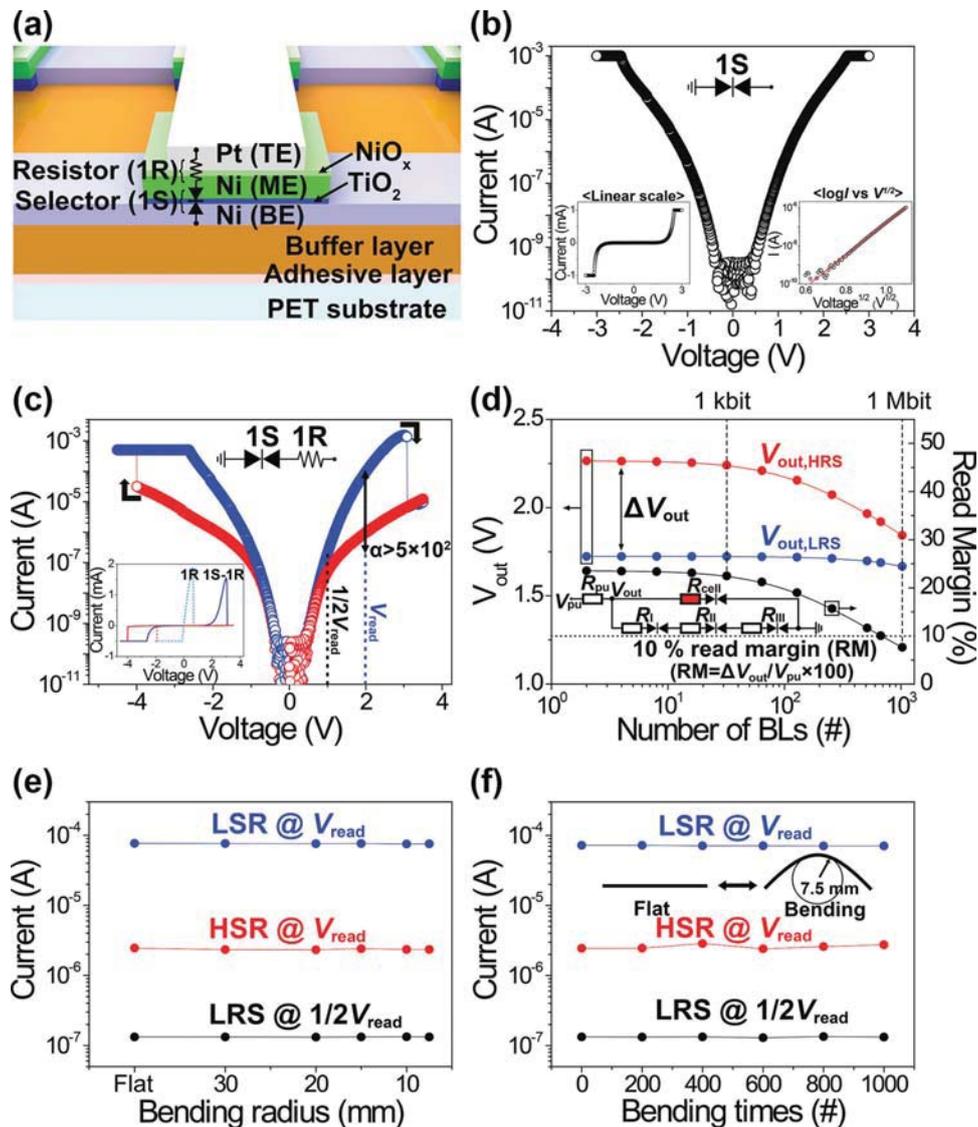


Figure 2. a) Schematic structure of a 1S–1R RRAM unit cell consisting of two electronic parts: a Ni/TiO₂/Ni selector (1S) and NiO_x-based resistive switching materials (1R). b) Non-linear I – V characteristics of the selector on semi-logarithmic and linear (left inset) scales with its circuit diagram. The right inset presents a Schottky emission fitting of $\log I$ versus $V^{1/2}$ in the positive voltage region. c) I – V characteristics of a 1S–1R unit cell in the DC sweep mode on a plastic substrate and the related circuit diagram. The inset shows the non-linear I – V characteristics of a 1S–1R cell on a linear scale in comparison with a 1R cell without a selection device. d) Calculated read margin as a function of the number of bit-lines in the 1S–1R crossbar array using one bit-line pull-up (OBPU) scheme with the corresponding circuit diagram to the OBPU scheme; a pull-up voltage (V_{pu}), a pull-up resistor (R_{pu}), a selected cell resistance (R_{cell}), and unselected cell resistances (R_i , R_{ii} , R_{iii}). e) The resistance values of HRS and LRS as a function of bending radius. f) Continuous bending fatigue test results for the 1S–1R cell up to 1000 iterations of bending and unbending. The inset shows a schematic illustration for repeated bending deformations (bending and release states) at the fixed bending radius of 7.5 mm.

effectively minimized in the 1S–1R device, in contrast to the 1R device, since half-selected cells in the cross-point structure, where half of the reading voltage is applied, mainly contribute to the sneak current.^[22,32,41]

To theoretically evaluate the enhancement of reading operation of the 1S–1R memory device, the read margin in the crossbar array using a "one bit-line pull-up" (OBPU) scheme^[31] is calculated in Figure 2d. For analyzing the read margin, the I – V curve of the 1S–1R unit cell was fitted using the Schottky emission equation in the low-voltage region (<1 V) and a ninth-degree polynomial fitting curve in the high-voltage region.

Based on the fitting curve, the numerical solution of the Kirchhoff equations was obtained using MATLAB (see the SI (Figure S5,S6) for details on the analysis of the read margin of the 1S–1R crossbar array). The simplified equivalent circuit of the 1S–1R crossbar array using the OBPU scheme is depicted in the inset of Figure 2d. Herein, the read margin ($RM = \Delta V_{out}/V_{pu}$, where $\Delta V_{out} = V_{out,HRS} - V_{out,LRS}$) criterion for determining the maximum crossbar array size is set to at least 10% of the pull-up voltage (V_{pu}); $V_{out,HRS}$ and $V_{out,LRS}$ represent the output voltages at the HRS and LRS, respectively.^[32] Compared to the 1R device,^[23] the calculated maximum array size with at

least 10% read margin dramatically increased up to 6.7×10^2 (450 kbits), indicating the feasibility of the fabricated flexible 32×32 1-kbit 1S–1R memory.^[32] The maximum array size could increase further to about tens of megabits by using an all bit-line pull-up (ABPU) scheme^[31,32] or by modulating the tunneling barrier.^[22,46] It has been especially difficult to achieve the selector with an engineered energy barrier on flexible substrates due to the necessity of high-temperature processes to modulate the energy barrier.^[22,46] We believe that our ILLO technology would allow high-temperature processing for such high-density flexible memories on plastic substrates.

The mechanical reliability of the flexible 1S–1R memory on a plastic substrate was evaluated for flexible electronic applications through bending tests as a function of bending radius and cycles (Figure 2e,f). Figure 2e shows the typical current values on half-cylindrical molds having various bending radii. The 1S–1R memory retains a consistent resistance ratio between the HRS and LRS without significant degradation to the bending radius of 7.5 mm [which corresponds to the surface strain ($\epsilon = t_s/2 \cdot r$, where t_s is the thickness of the substrate and r is the bending radius)^[6,47] of 0.33%]. At a curvature radius of 5 mm (corresponding to a strain of 0.5%), cracks and electrical shorts on the device began to be observed. However, we believe that additional improvements would be possible by adopting ultrathin substrates^[2,48] or encapsulation techniques such as a mechanical neutral space.^[49]

As shown in Figure 2f, the device has good mechanical stability during 1000 iterations of bending, which demonstrates the excellent mechanical robustness of the flexible RRAM (see the SI for bending tests with 10 cells, Figure S7). This outstanding mechanical stability benefits from the epoxy passivation layer,^[33] which improves mechanical stability during bending and also prevents laser-induced fractures during the ILLO process.

In order to characterize the reliability of the flexible 1S–1R RRAM, endurance and retention tests were performed under repeated voltage pulses. The upper graph of Figure 3a shows the electrical response of the 1S–1R memory to the input voltage pulses. The initial resistance state is set to the HRS and switched from the HRS to the LRS by applying the voltage pulse of -4.5 V. The LRS is retained during half of the reading voltage ($1/2V_{\text{read}} = 1$ V) and the reading voltage ($V_{\text{read}} = 2$ V); the non-linear I – V characteristics can also be observed in pulse mode. The resistance state is converted to the HRS by applying a voltage pulse of 3.5 V, and the resistance state is preserved at half of the reading voltage ($1/2V_{\text{read}}$) and the reading voltage (V_{read}). The resistance switching by voltage pulse occurs stably and consistently for more than 100 cycles (Figure 3a, lower). The retention characteristics of the 1S–1R device were also assessed on an iterated reading voltage of 2 V and on half of that at room temperature, indicating the 1S–1R device not only has superior retainability for stored data but also non-linearity up to 2×10^4 s, as presented in Figure 3b.

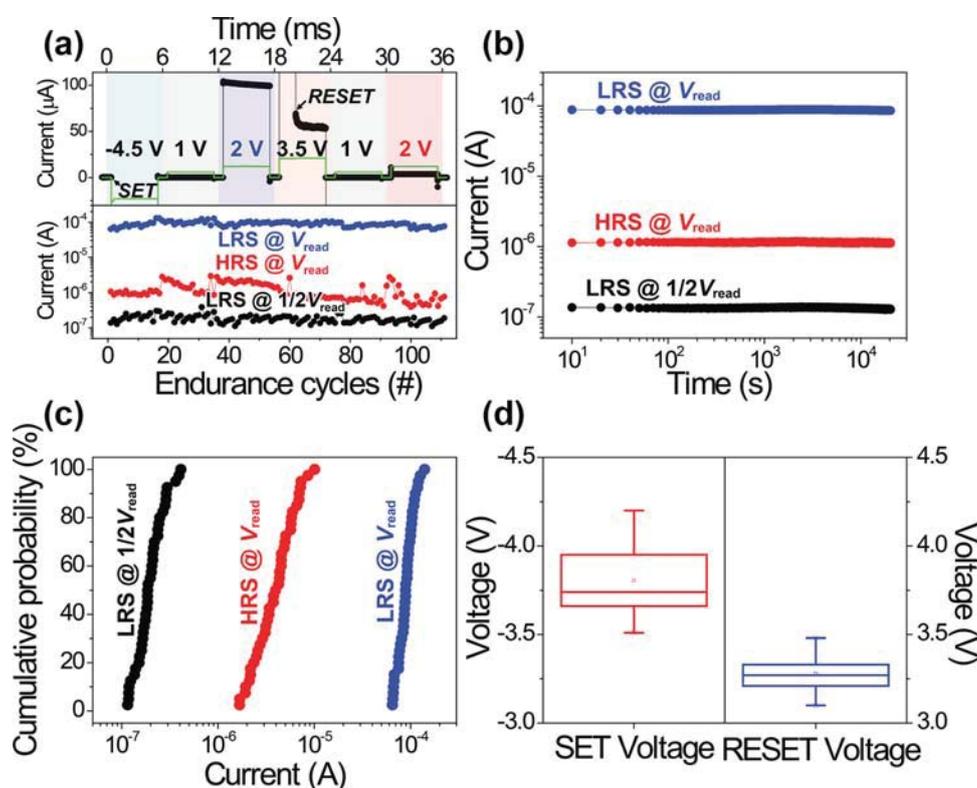


Figure 3. a) Electrical responses to input voltage pulses (upper graph) and endurance test data of 1S–1R RRAM (lower graph) conducted by repeated voltage pulses. b) Retention property of the RRAM at V_{read} and $1/2V_{\text{read}}$. c) Cumulative probability data of the HRS and LRS at V_{read} and $1/2V_{\text{read}}$ obtained from the I – V curves of 40 unit cells. d) SET and RESET voltage distributions of the RRAM depicted by a box-whisker plot obtained from I – V curves of 40 unit cells.

Statistical analyses to examine operational uniformity were performed on 40 unit cells, and the results are presented in Figure 3c,d. Figure 3c shows the cumulative probability of the current at V_{read} and $1/2V_{\text{read}}$ obtained from I - V curves of 40 unit cells. The HRS and LRS exhibit a narrow distribution without current overlap at both V_{read} and $1/2V_{\text{read}}$. Figure 3d shows the SET and RESET voltage distribution of the flexible 1S-1R RRAM depicted by a box-whisker plot obtained from I - V curves. The programming voltage margin between the SET and RESET was stabilized by the integrating selection device, compared to a 1R device.^[7] This result shows that the integrated selector plays two important roles; it acts as a selection device preventing cell-to-cell interference and as a buffer resistor to suppress excessive current flow during the SET/RESET process.^[7,44,50] Interestingly, both the HRS and SET voltage exhibit slightly wider distributions in the cumulative probability of current and voltage distribution. This is presumably because of the variation of the ruptured filament path length.^[21]

The important functions of the integrated selectors in the crossbar array are depicted in Figure 4a. For the reading process in the worst-case scenario, an OBPU scheme^[31] is considered here: a selected one bit-line is pulled up to a voltage of 2 V with a grounded word-line, while all other lines are being floated. In this OBPU scheme, applied voltage on the selected bit-line results in a total voltage drop of 2 V across the selected devices

in the HRS, whereas the voltage drop of the surrounding cells, sharing the selected word- and bit-line, is lower than 1 V.^[22,51] By integrating selectors with resistive memory, the current flowing through these half-selected cells can be exponentially suppressed due to the non-linear current characteristics of the selectors.^[32]

Figure 4b presents the actual addressing test data of a 3×3 1S-1R device in the worst-case scenario with a color map based on the current flowing, showing that the integrated selectors effectively suppress unintended current paths. This addressing test was conducted using a Keithley 4200-SCS semiconductor characterization system with six probes, connected to one grounding unit and a five-source-measurement unit (SMU). These results will be extended to multiple $n \times n$ memory cells by integrating the additional peripheral circuits with the crossbar memory array.^[5,31] To verify the accurate addressing of flexible 1S-1R memory, additional tests under various conditions were performed. Figure 4c shows the results of addressing tests based on the current of the LRS (logic state "1") and the HRS (logic state "0") with a 3×3 image representing "KAIST". Although there are some fluctuations in the HRS, the results clearly demonstrate the 1S-1R memory can work efficiently on a plastic substrate without electrical interference by integrating selectors with each memory cell.^[4,23]

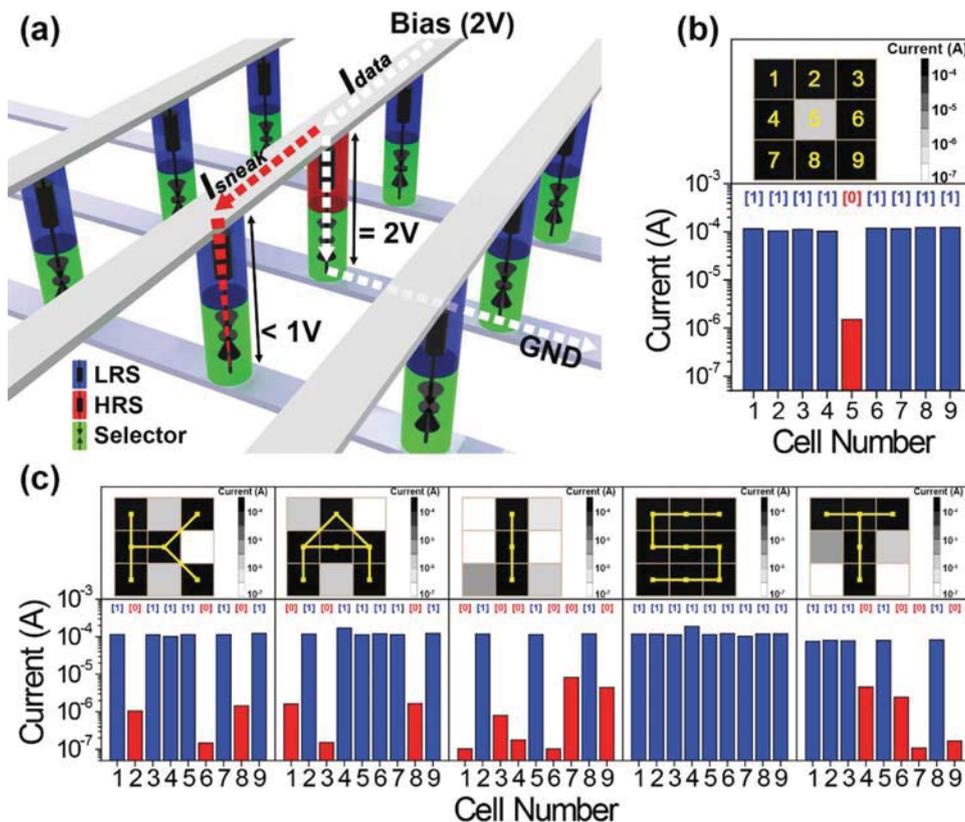


Figure 4. a) Schematic illustration of the role of the integrated selector in the crossbar memory array in a reading process using the OBPU scheme. Sneak path currents (I_{sneak}) flowing through half-selected cells, which are represented by red dashed lines, are suppressed due to the non-linear current characteristics of the integrated selector. This is in contrast with a correct data signal (I_{data}) flowing through a selected cell to the ground (GND) marked by white dashed lines. b) The histogram of currents of 3×3 1S-1R crossbar-structured memory and the corresponding color map under the worst-case scenario. c) Addressing test results expressed by the histograms of currents with 3×3 images representing "KAIST".

In summary, we have introduced a methodology to fabricate fully functional flexible memory with a 32×32 1S–1R array for high packaging density. The ILLO process utilized herein enabled the crossbar-structured memory processed on a rigid substrate using conventional micro-fabrication over large area to be transferred onto a flexible substrate without any mechanical failure. Inorganic substances employed in the study, including the exfoliation, buffer oxide, and device layers, can enable the high-temperature processing, which was previously difficult to achieve on conventional plastic substrates such as the modulation of tunneling barrier^[22,46] to enhance the performance of selector. The developed flexible device demonstrated reliable and reproducible resistive switching with excellent mechanical stability on a plastic substrate. Finally, addressing tests verifying the absence of electrical interference were successfully performed under various conditions, writing symbolized letters on a plastic substrate. The proposed approach using the ILLO could open a facile and robust strategy for fabricating flexible non-volatile memory devices with high packaging density, and possibly extending further to the realization of SoP. We are currently investigating flexible nanoscale devices that are processed at extremely high temperature in hopes of enhancing performance and packaging density.

Experimental Section

Fabrication of One Selector–One Resistor Resistive Memory: The Ni BEs were patterned using a RF sputtering and lift-off process. The TiO_2 (10 nm) was deposited on Ni BEs using 80 cycles of thermal atomic layer deposition at a substrate temperature of 80 °C. Tetrakis(dimethylamino)titanium ($\text{Ti}(\text{N}(\text{CH}_3)_2)_4$, TDMAT) and H_2O were used as the Ti precursor and oxygen source, respectively. The cycle sequence was TDMAT (1 s), Ar (20 s), H_2O (1.5 s), and Ar (20 s). The square-shaped Ni MEs were formed in the same way as the BEs. A nickel oxide layer was formed on the Ni ME by a plasma oxidation process in an inductively coupled plasma–reactive ion etching (ICP-RIE) system with a RF power of 200 W for 5 min at room temperature. After formation of the nickel oxide layer, the Pt/Ti (250 nm/10 nm) were deposited as the TE.

Electrical Measurements: Electrical characterization and evaluation were performed using a Keithley 4200-SCS (DC voltage/current sweep), a Keithley 4225-PMU (pulse generator and waveform capture of voltage/current), and a 4225-RPM (remote amplifier/switches).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the Basic Science Research Program (grant code: NRF-2012R1A2A1A03010415, CAFDC/Keon Jae Lee/No. 2007-0056090) funded by the Korean government (MSIP) through the National Research Foundation of Korea (NRF).

Received: June 3, 2014

Revised: July 15, 2014

Published online: September 8, 2014

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