ACF-Packaged Ultrathin Si-based Flexible NAND Flash Memory

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Abstract

In this paper, we demonstrate an ACF-packaged ultrathin Si-based flexible NAND flash memory by adopting a simple method, without using a conventional transfer process. By gently etching the bottom sacrificial silicon of the SOI wafer, flip-chip bonded devices were sufficiently thinned down (roughly to 1 μm) to fabricate highly flexible, fully packaged Si-based NAND flash memory, without any cracks or wrinkles. The work presented here suggests a useful methodology to realize various high-performance, fully packaged Si-based flexible LSI devices.

Introduction

Recently, flexible electronics have attracted increasing attention thanks to their combination of low weight, high portability, low fragility, and variable structure, offering considerable improvements over the weaknesses of conventional rigid electronics. [1] In particular, the development of electronic devices such as flexible processors and memories are considered crucial to address the increasing demands of data processing, information storage, and network communications. [2] Although many studies on flexible devices have utilized organic and polymeric materials, they typically exhibit insufficient performance due to inherent material properties, and their low degree of integration has been problematic. In this respect, silicon-based flexible large-scale integration (LSI) devices have been considered promising candidates for next-generation flexible non-volatile memory devices, due to their outstanding performance, high density capability, and compatibility with state-of-the-art semiconductor processes. [3] Although our group previously demonstrated ultrathin Si-based flexible radio frequency integrated circuits (RFICs) fabricated with 0.18 μm CMOS process, [4] significant challenges still remain in developing Si-based flexible memory devices, including how to stably realize flexible LSI on plastics.

Another critical issue related to flexible and wearable electronics is the packaging process, which provides key functions such as signal interconnections, mechanical protection, and power distribution. There have been substantial efforts to utilize anisotropic conductive film (ACF) as an elastic and resilient packaging material, and our group previously demonstrated a flexible GaAs light-emitting diode (LED) interconnected by ACF to a plastic substrate. [5] However, employing ACF with thin fragile silicon chips is limited by the high pressure required by the flip-chip bonding process. As a result, ACF packaged chips have remained relatively thick, up to tens of microns, in order to withstand the pressure, which therefore limits the flexibility of Si-based electronic devices.

Herein, we demonstrate an easy method for fabricating ultrathin Si-based flexible devices with the electrical interconnections necessary for practical flexible applications, by employing a flip-chip bonding technique and subsequent wafer thinning process. Also, a fully packaged ultrathin Si-based flexible NAND flash memory was successfully fabricated and analyzed.

ACF-Packaged Si-based Flexible Device Fabrication

Fig. 1 illustrates the fabrication method of the ACF-packaged Si-based flexible NAND flash memory. (i) A high performance NAND flash memory is constructed on the top-Si layer (400 nm) of the SOI wafer by conventional semiconductor fabrication processes. (ii) Interconnection between the fabricated device and the flexible substrate was made by flip-chip thermo-compression bonding cycle with ACF. (iii) The sacrificial bottom silicon was completely removed by aqueous alkaline potassium hydroxide (KOH) solution. In this case, the buried oxide (BOX) layer acts as the etch stop, leaving the thin, uniform device layer after the wet etch. (iv) Finally, the fully packaged ultrathin Si-based flexible NAND flash memory was fabricated with electrical interconnections.

In light of previous studies on various flexible device fabrication techniques, it is important to note that this particular method has several distinct advantages. In the first place, this method utilizes a single crystalline silicon piece, which is particularly compatible with the full-chip scale complementary metal oxide semiconductor (CMOS) process. In addition, the highly thinned chip is capable of high flexibility which makes the total device resilient under various stress conditions. Moreover, this approach provides direct interconnection between the device and the outer electrode for practical use without requiring an additional wiring process. More importantly, there is no need to transfer the Si device to a flexible substrate, as demonstrated in previous works, [6] since the flip-chip bonded device is already strongly attached to the flexible printed circuit board (FPCB) substrate. Therefore, our approach enables one to fabricate ultrathin Si-based flexible devices with high yield.

Fig. 2 shows a photograph of the ACF-packaged ultrathin Si-based flexible NAND flash memory wrapped on a glass rod (3.5 mm radius). The highly flexible characteristics of the developed device are presented in the inset of Fig. 2. Optical microscope (OM) images of the NAND flash active area (Fig. 3) and the electrode area (Fig. 4-5) indicate they have no cracks or wrinkles.

Mechanical Properties of the Fabricated Device

Fig. 6 shows a photograph of the ACF-packaged ultrathin Si-based flexible chip used for electrical measurement (left) and a magnified top-view image of the 144-series daisy-chain (right). No mechanical defects were observed in spite of the existing electrode bump, even after repetitive bending. Fig. 7

presents a cross-sectional scanning electron microscopy (SEM) image of the ultrathin Si device interconnected with the flexible substrate. A captured conductive filler ball, which is the effective current path, was confirmed through these images.

Figs. 8-10 show the interconnection test results as a function of bending radii and bending cycles. No significant increase in contact or daisy-chain resistance was observed until the chip was bent to 2.5 mm and 2 mm radius, respectively. In addition, as shown in Fig. 10, the interconnection also exhibited good mechanical endurance during a bending fatigue test involving 3×10^5 iterations (5 mm radius). The observed outstanding mechanical and electrical flexibility are mainly attributed to the resilience of the packaging material (ACF) and the ultrathin Si chip.

Flash Memory Cell Operation

The usefulness of the introduced method was demonstrated by fabricating a Si-based flexible NAND flash memory, and it is worth noting that it could also be applied to a CMOS processed integrated device. Fig. 11 shows a photograph of the ultrathin Si-based flexible flash memories, which are interconnected with the flexible substrate. The developed flash memory cells have a channel length of 15 μm, and a channel width of 250 μm. The inset of Fig. 11 shows a cross-sectional transmission electron microscopy (TEM) image of $Al_2O_3/Si_3N_4/Al_2O_3$ multilayer thin films deposited on the silicon for the Si-based flash memory application.

Fig. 12 shows the charge trap memory characteristics of the ultrathin Si-based flexible flash memory. Voltage pulses of -16 V/0.5 s were applied at the gate for erasing in order to obtain double transfer curves with increasing maximum gate voltages. As shown in Fig. 12, a higher programming bias applied at the gate results in a wider memory window, indicating that more electrons are collected in the trap site according to the increased program bias. Vth shift was obtained with respect to the voltage pulse width, from 5×10^{-7} s to 10 s at an applied bias of + 12 V (programming) and -16 V (erasing), as shown in Fig. 13. The threshold voltage shift increased with increasing erase/program operation time width.

To demonstrate the operation of the NAND flash memory, an erased and programmed cell were set to a negative and positive threshold voltage, respectively. In order to meet this condition for Vth distribution, our flash memory device was erased by voltage pulses of - 16 V/0.5 s, and programmed by a voltage pulse of 12 V/0.5 s. Fig. 14 shows the typical program/erase operation for the NAND flash memory. The transfer curves of programmed and erased states were measured at $V_d = 0.5$ V, and the memory device exhibited a high ON/OFF at $V_g = 0$ V (reading voltage for a selected memory cell in the NAND logic gate).

Fig. 15 shows the endurance test results of the flexible flash memory, which indicated a stable and reversible switching cycle property for more than 2000 cycles, with a high Ion/Ioff of > 10^2. A retention test was also assessed to evaluate non-volatile data storage ability in the programmed and erased states. As shown in Fig. 16, the flexible flash memory device has stable retention characteristics up to 10^4 s at room temperature.

NAND Flash String Operation

Fig. 17 shows the cross-sectional schematic illustration (upper) and the operation conditions of the flexible NAND flash memory (lower). The Si-based flash memory was assembled into a series string of 8 memory cells to constitute a NAND flash memory array. Fig. 18 shows the string current of the NAND flash string according to the address number of memory cells. As shown in Fig. 18, there was a distinct difference in the string current between programmed and erased cells.

To examine the uniformity of the flexible NAND flash memory, a color map illustrating the memory state of the 64 cells in the 8 × 8 array is presented in Fig. 19. To confirm the data storage ability of our memory device, ASCII character code was used in the writing process to represent the letter 'KAIST MSE' according to a string number that corresponded to the 8-bit binary ASCII character codes. As shown in Figs. 19-20, the string current distribution demonstrates excellent separation with a ratio of more than 20, and our memory device provides the ability to save desired ASCII character codes, which is essential in the application of a non-volatile memory device.

Figs. 21-22 show that the flexible NAND flash memory retains its string current ratio between the erased and programmed states without any degradation during bending tests. These results demonstrate that our fabricated ACF-packaged Si-based flexible NAND flash memory provides good mechanical stability.

Conclusion

In summary, a highly flexible ACF-packaged ultrathin Si-based NAND flash memory was fabricated. The device demonstrated reliable and reproducible memory operation with excellent mechanical stability on a flexible substrate. Finally, addressing tests, including writing symbolized letters, were successfully performed under various conditions. The proposed method can potentially open a facile and robust strategy for fabricating various fully packaged Si-based flexible memory devices. Additionally, we are currently developing a roll-to-roll process which will allow the mass production of fully packaged Si-based LSI devices on flexible substrates.

Acknowledgements

This work was supported by the internal research program "Development of Infrastructure for Flexible Devices with High-performance Using Nanomaterials (SC1090)" of Korea Institute of Machinery and Materials, and the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054193).

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[2] S. Kim et al., *Nano Lett.*, **11**, p. 5438, 2011.
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[5] C. Jeong et al., *Energy Environ. Sci.*, **7**, p. 4035, 2014.
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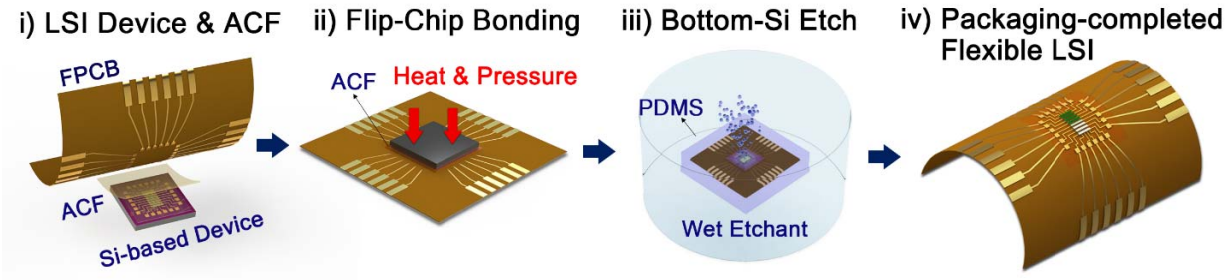


Fig. 1. Fabrication procedure of the ACF-packaged ultrathin Si-based flexible LSI device. (i) Device fabrication on the top-Si of the SOI wafer, by conventional semiconductor process. (ii) Interconnecting the device and the flexible substrate (FPCB) by flip-chip thermo-compression bonding cycle with ACF. (iii) Removing the bottom sacrificial silicon by aqueous alkaline potassium hydroxide (KOH) solution. (iv) Finally, the ACF-packaged ultrathin Si-based flexible device was fabricated with electrical interconnection for practical use.

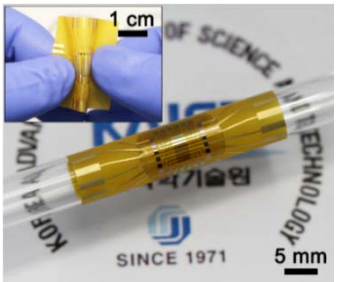


Fig. 2. Photograph of the fabricated ACF-packaged ultrathin Si-based flexible NAND flash memory wrapped on a glass rod (3.5 mm radius). The inset shows the highly flexible characteristics of the device.

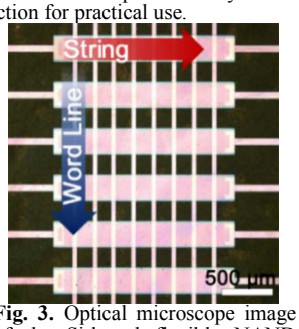


Fig. 3. Optical microscope image of the Si-based flexible NAND flash active area, with no cracks or wrinkles.

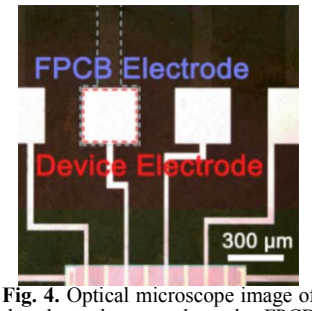


Fig. 4. Optical microscope image of the electrode area where the FPCB electrode and the device electrode are interconnected.

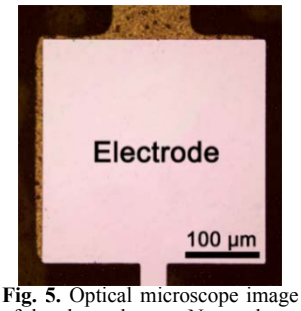


Fig. 5. Optical microscope image of the electrode area. No cracks or wrinkles were observed in spite of the height difference caused by the existing electrode bump.

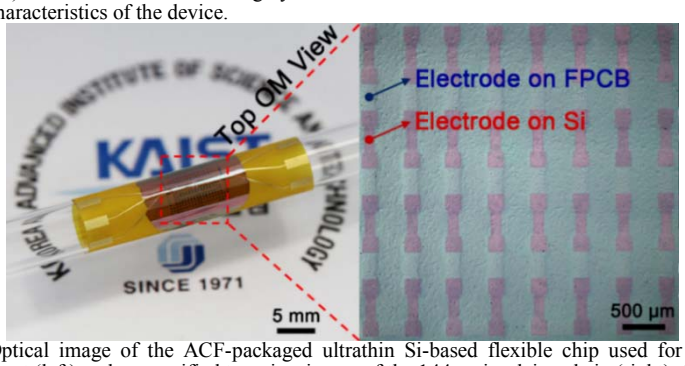


Fig. 6. Optical image of the ACF-packaged ultrathin Si-based flexible chip used for electrical measurement (left) and a magnified top-view image of the 144-series daisy-chain (right). (Electrode area = 1802 um2.)

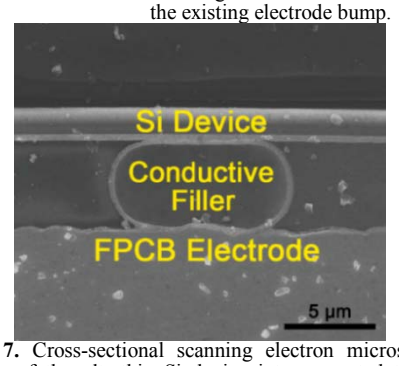


Fig. 7. Cross-sectional scanning electron microscopy image of the ultrathin Si device interconnected to the flexible substrate (FPCB) by a conductive filler ball.

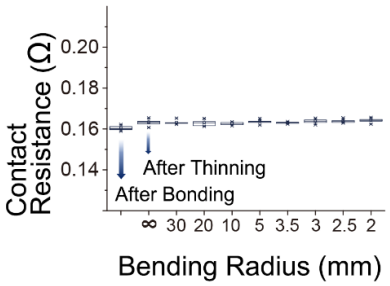


Fig. 8. Measured contact resistance with varying bending radius. No significant resistance increase was observed until it reached a 2 mm bending radius.

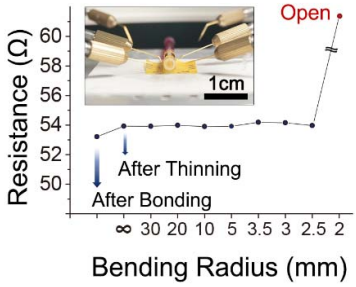


Fig. 9. Measured 144-series daisy-chain resistance with varying bending radius. (The slightly high initial resistance is caused by the resistance of the thin electrode fabricated on the Si chip rather than the interconnection resistance.) No significant resistance increase was observed until it was bent to a 2.5 mm bending radius.

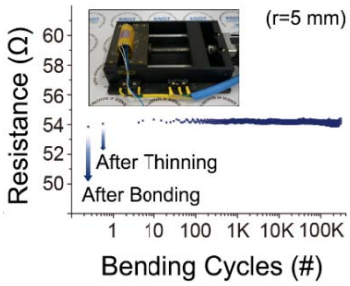


Fig. 10. Measured 144-series daisy-chain resistance with repetitive bending. No significant resistance increase was observed during 3×10^5 iterations (5 mm radius) of bending.

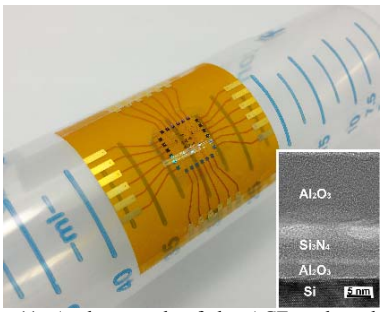


Fig. 11. A photograph of the ACF-packaged Si-based flexible flash memories on flexible substrate. The inset shows a cross-sectional TEM image of the $Al_2O_3/Si_3N_4/Al_2O_3$ multilayer thin films deposited on the silicon to fabricate the flash memory.

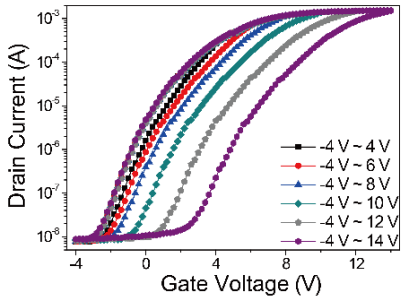


Fig. 12. The charge trap memory characteristics of the flexible flash memory. Voltage pulses of - 16 V/0.5 s were applied to the gate for erasing, in order to obtain double transfer curves with increasing maximum gate voltages.

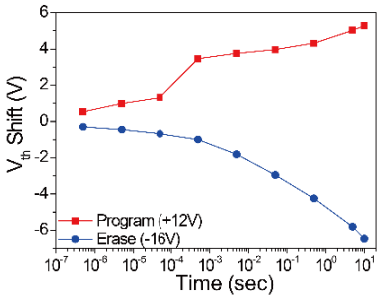


Fig. 13. The V_{th} shift plots of the flexible flash memory as a function of the voltage pulse widths. The V_{th} shifts were increased with increasing erase/program operation times.

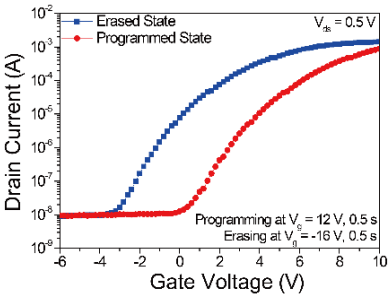


Fig. 14. The transfer curves of the programmed and erased states were measured at V_d = 0.5 V. This memory device exhibited a high on/off at V_g = 0 V (reading voltage for a selected memory cell in the NAND logic gate).

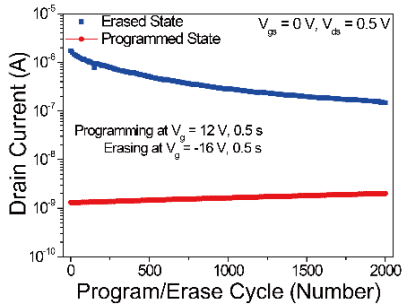


Fig. 15. Endurance test of the flexible flash memory measured during more than 2000 cycles.

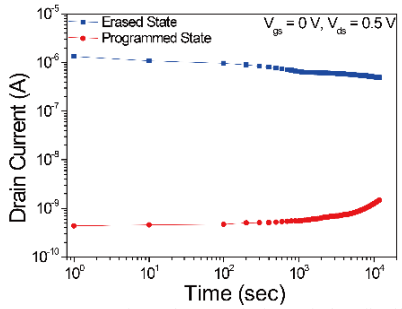
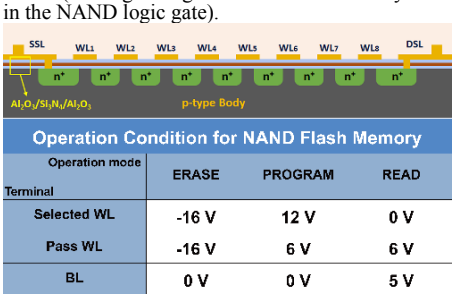


Fig. 16. Retention characteristics of the flexible flash memory..



Operation Condition for NAND Flash Memory

Operation mode / Terminal	ERASE	PROGRAM	READ
Selected WL	-16 V	12 V	0 V
Pass WL	-16 V	6 V	6 V
BL	0 V	0 V	5 V

Fig. 17. Schematic illustration of a cross-sectional view of a Si-based flexible NAND flash memory. The Si-based transistors with $Al_2O_3/Si_3N_4/Al_2O_3$ stacks have been assembled into a series string of 8 memory MOSFETs. Operation conditions for the NAND flash cell string are presented below.

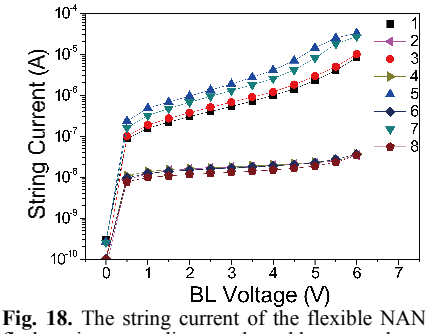


Fig. 18. The string current of the flexible NAND flash string according to the address number of memory cells. There is a distinct difference in the string current between the programmed and erased cells.

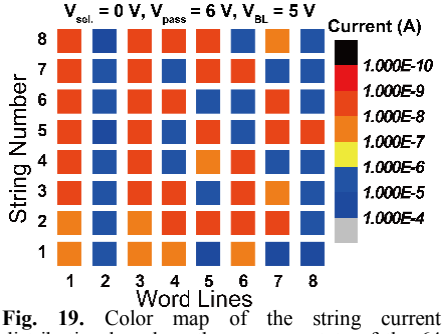


Fig. 19. Color map of the string current distribution based on the memory state of the 64 cells in the 8 x 8 array. To verify the string current difference between erased and programmed states, the read operation was carried out with V_{sel} = 0 V, V_{pass} = 6 V, and V_{BL} = 5 V.

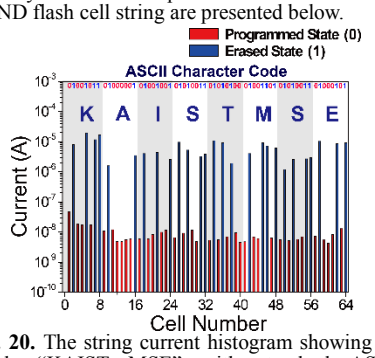


Fig. 20. The string current histogram showing the words "KAIST MSE" with standard ASCII characters within the 64 bit flexible NAND flash memory.

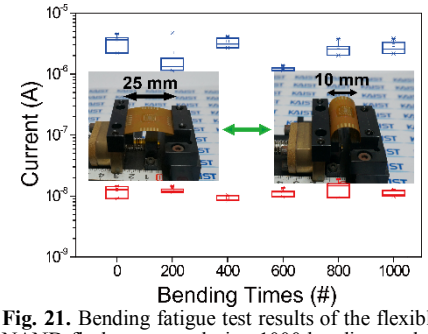


Fig. 21. Bending fatigue test results of the flexible NAND flash memory during 1000 bending cycles. The inset shows photographs of the bending and unbending states.

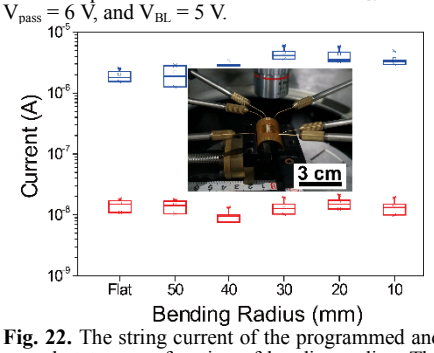


Fig. 22. The string current of the programmed and erased states as a function of bending radius. The inset is a photograph of the string current measurement under a flexed condition.